Wistron-SKLU Schematics
Brook_SLU

2015-06-29
REV : -1M

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

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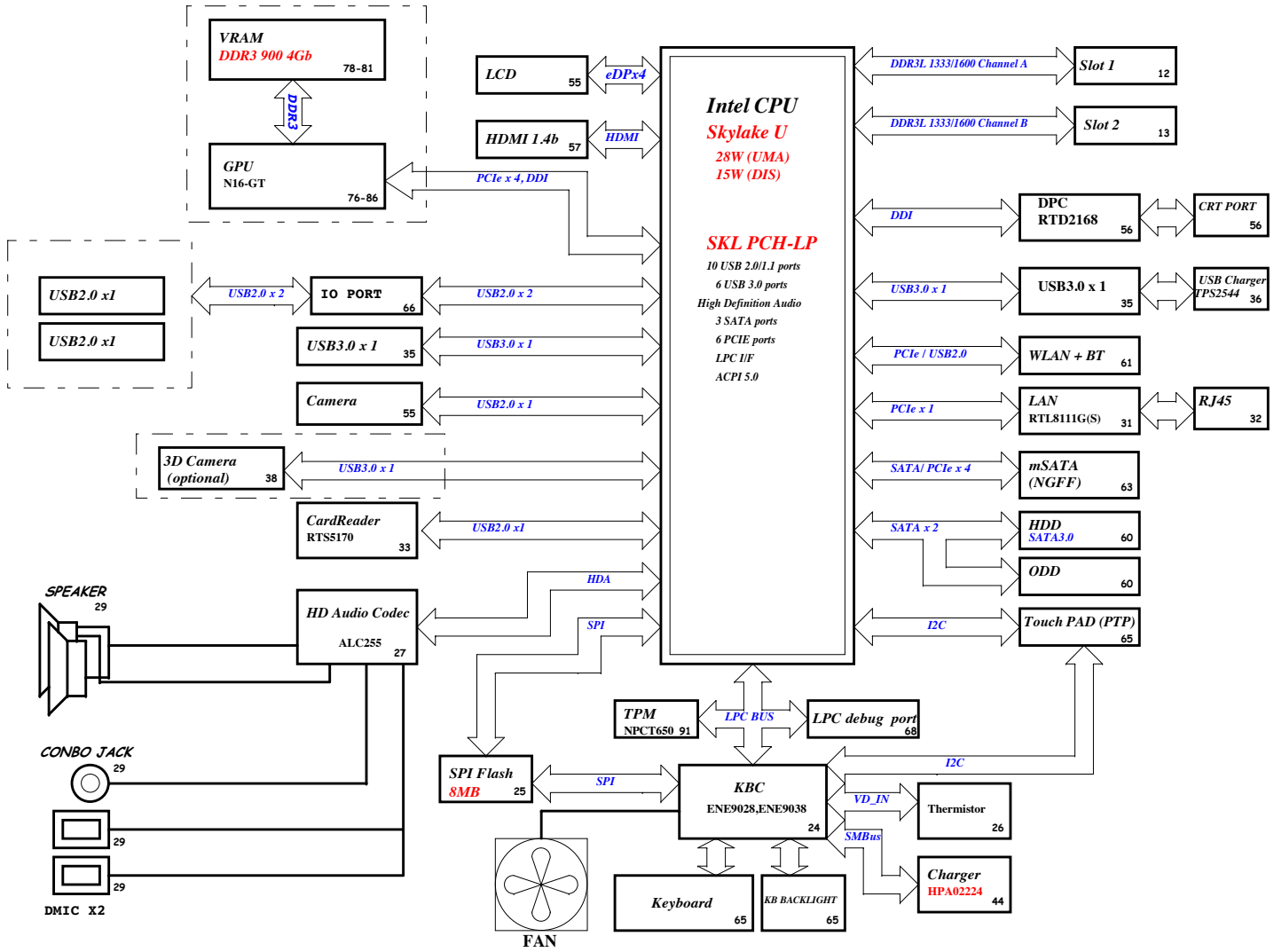
Project code:
Brook SL 17 --> 4PD058010001
PCB P/N:14277
Revision: SC



CHARGER HPA02224RGRR-1-GP 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT6575D 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power ISL95813HRZ-GP 46,47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR3L SUS RT8231AGQW-GP 51	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

CPU 1D0V_S5 RT8231AGQW-GP 52	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

CPU 1.8V_S5 RT8068AZQWID-GP-U 53	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S5

Switches 40	
INPUTS	OUTPUTS
1D8V_S5	1D8V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1V_S5	1V_VCCIO
	1V_VCCST

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal

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Title: **Block Diagram**

Size	Document Number	Rev
C	Brook_SLU	1M

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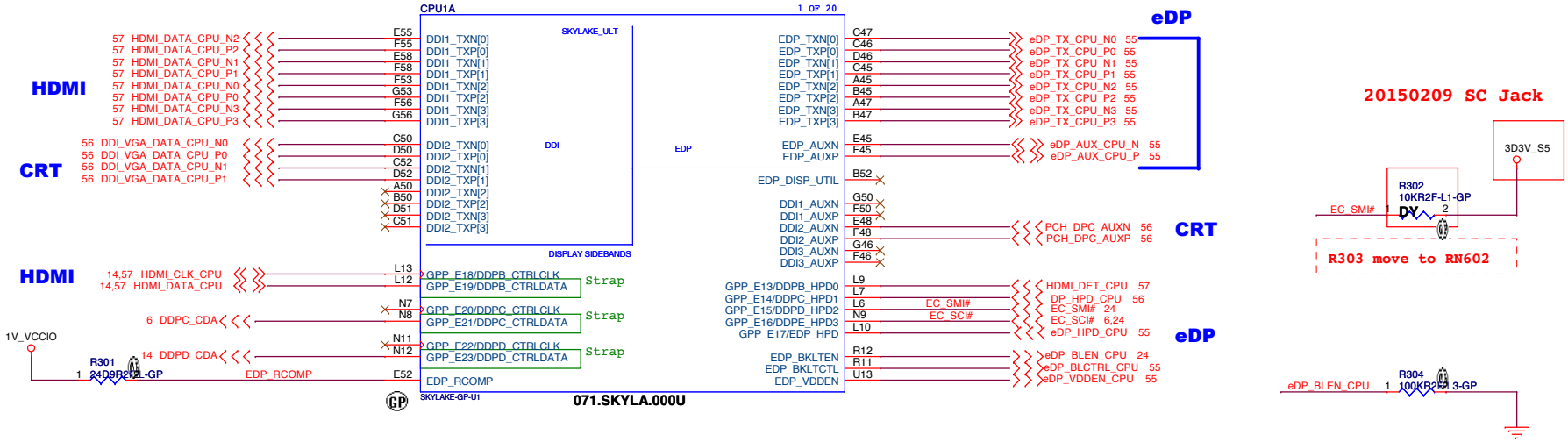
Main Func = CPU



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

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Title: *CPU_(DISPLAY)*

Size: A3 | Document Number: Brook_SLU | Rev: 1M

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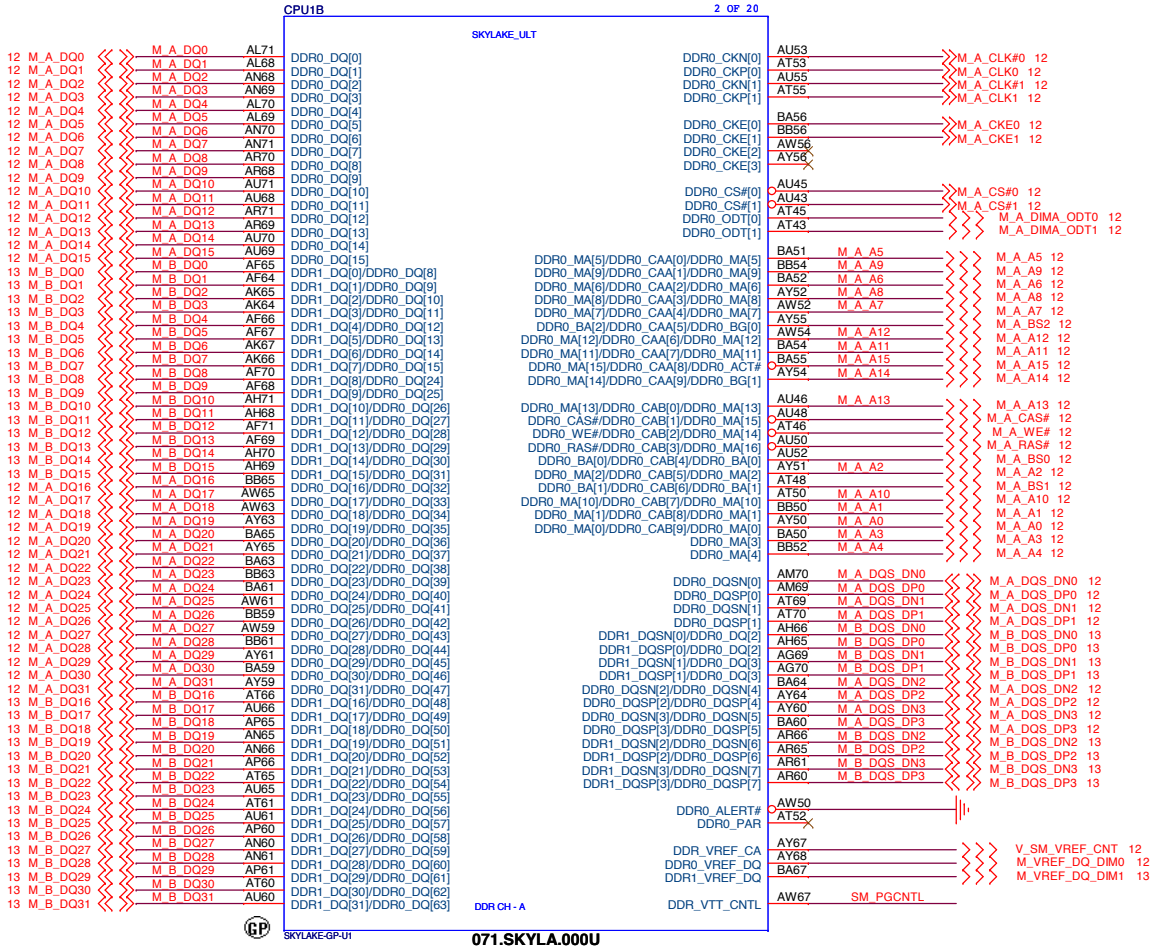
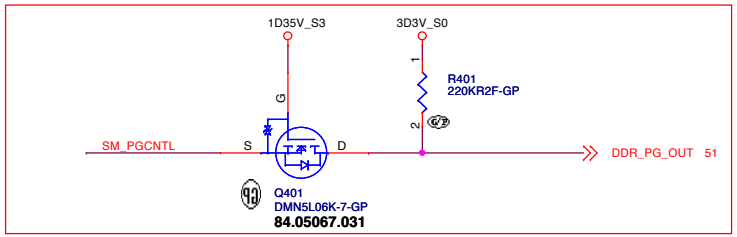
Main Func = CPU

DDR3L ball type: Interleaved Type





2nd = 084.00138.0A31

20141023 Jack

<Core Design>

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Title	CPU_(DDR)
Size A3	Document Number Brook_SLU
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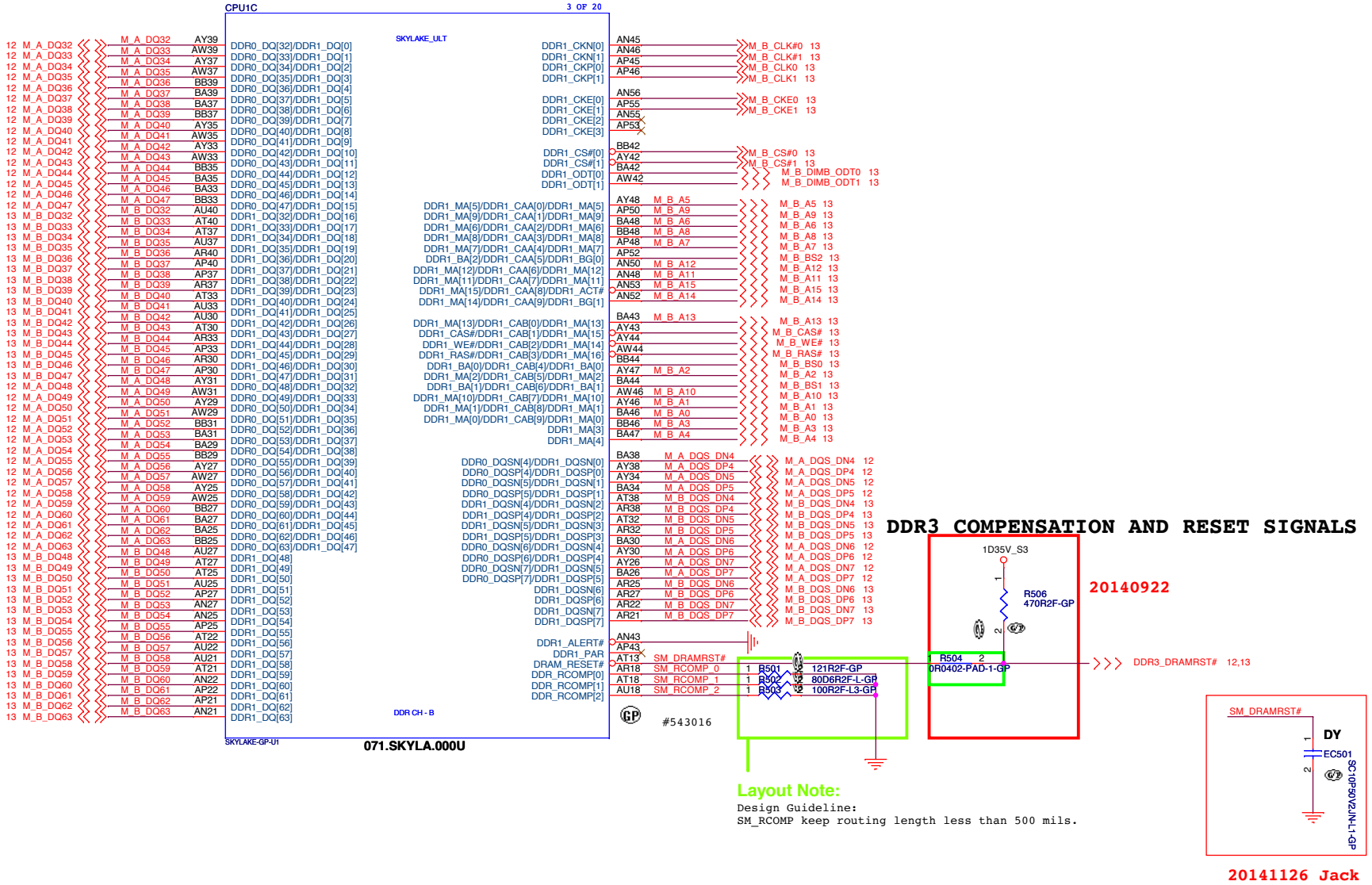
Main Func = CPU



Layout Note:

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

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Title	*CPU_(DDR)*
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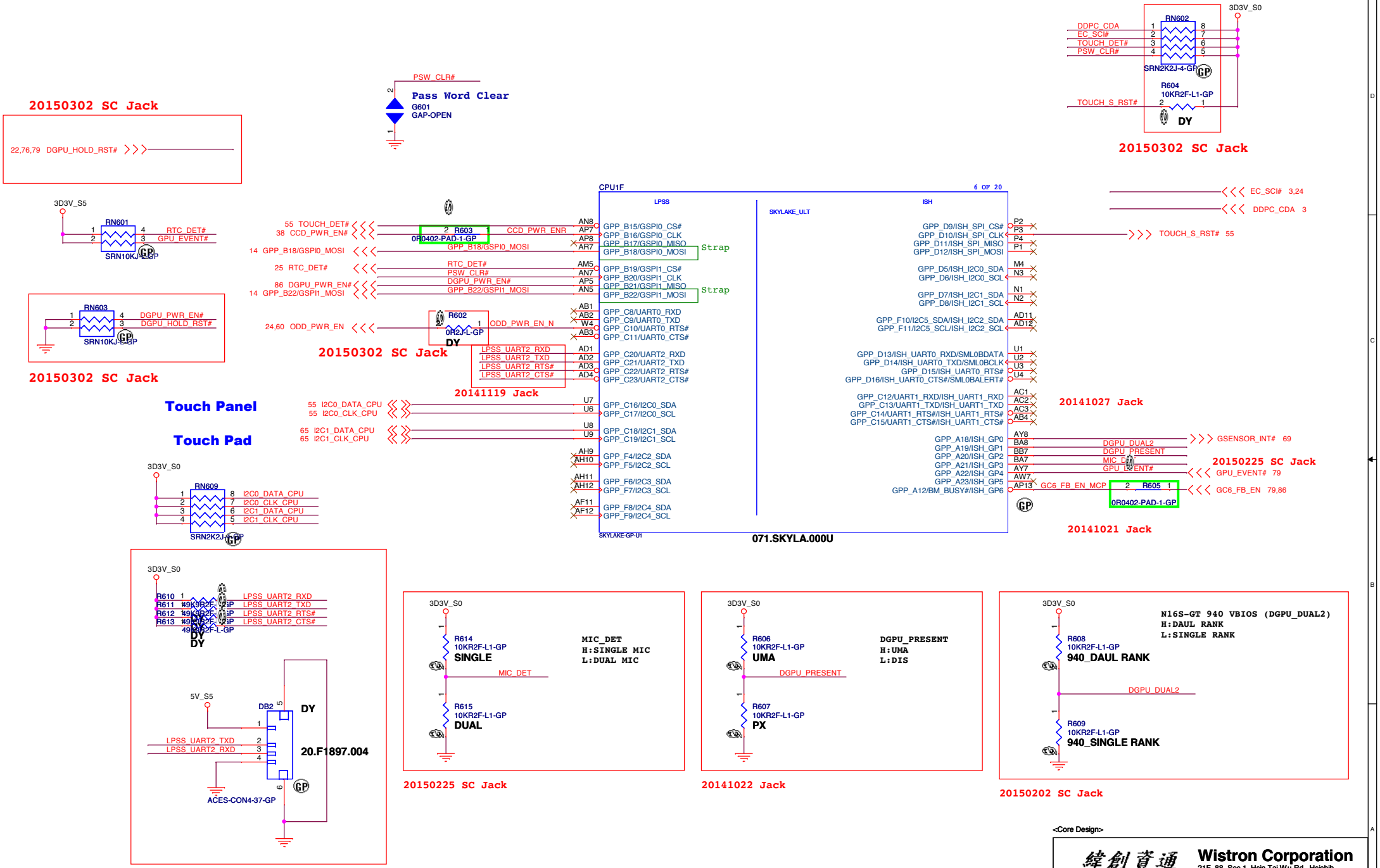
Main Func = PCH



<Core Design>

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Title: CPU_(LPSS/ISH)

Size: A3 | Document Number: Brook_SLU | Rev: 1M

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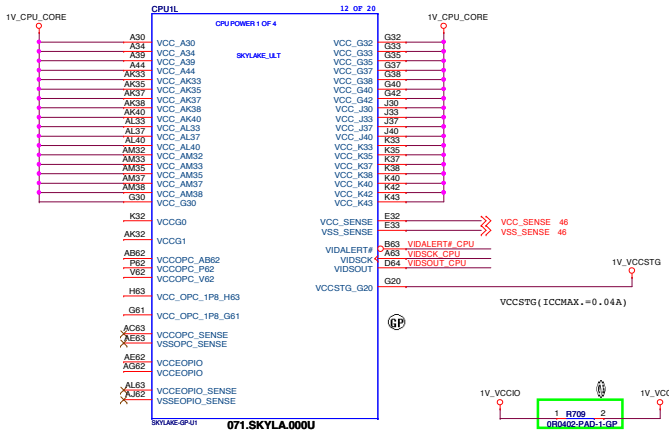
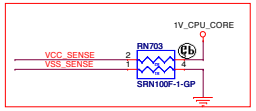
Main Func = CPU

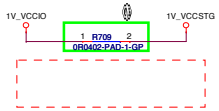


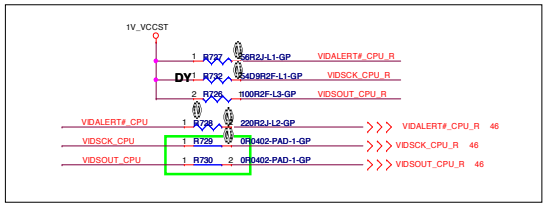


20150302 SC Jack

Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil





CLOSE CPU

SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

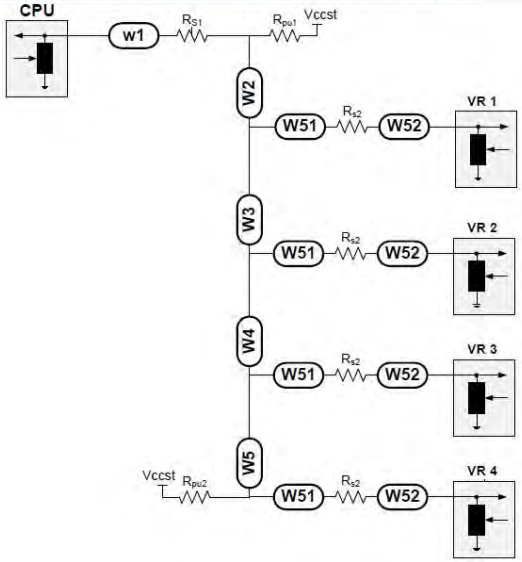


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{GT} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

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Title: **CPU_POWER1**

Size: A2 | Document Number: Brook_SLU | Rev: 1M

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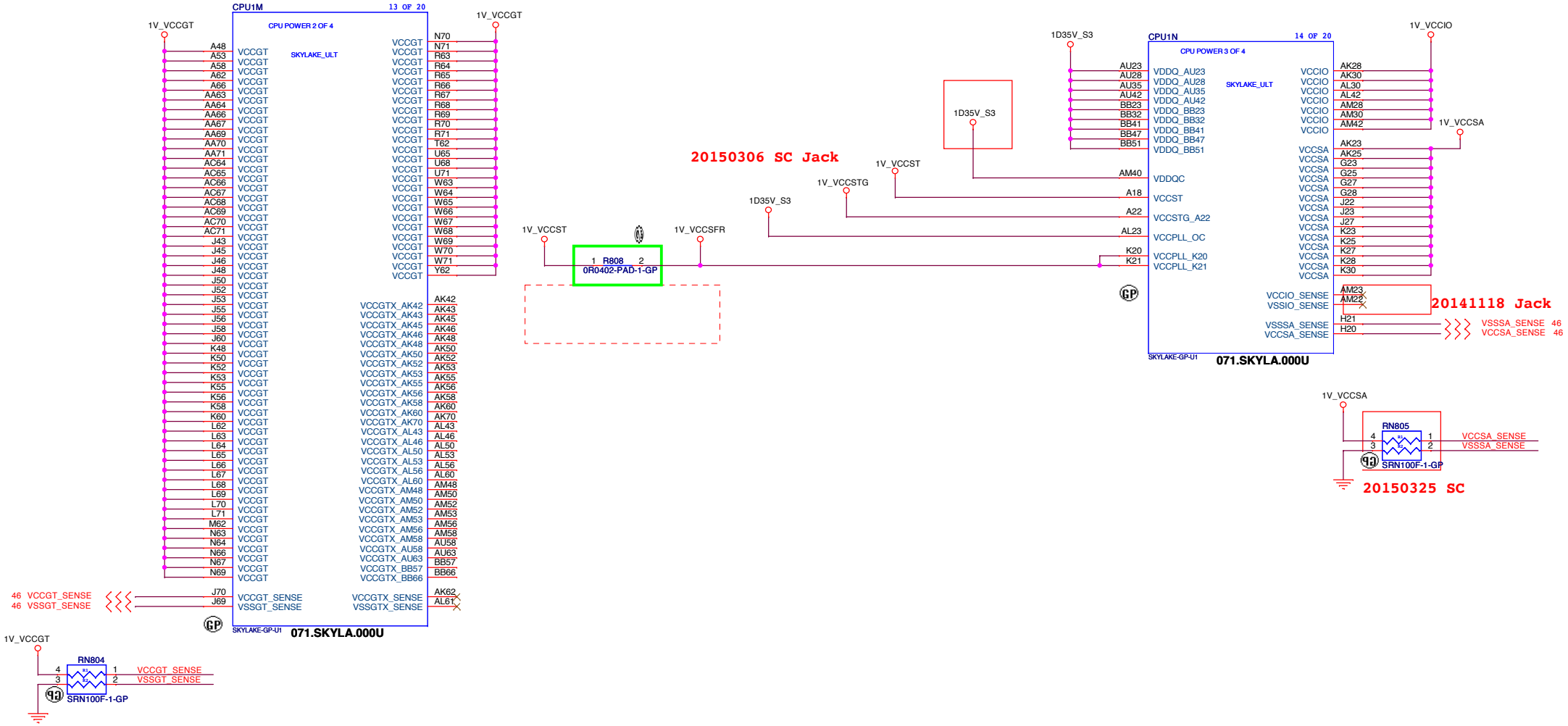
Main Func = CPU



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Title: ***CPU_POWER1***

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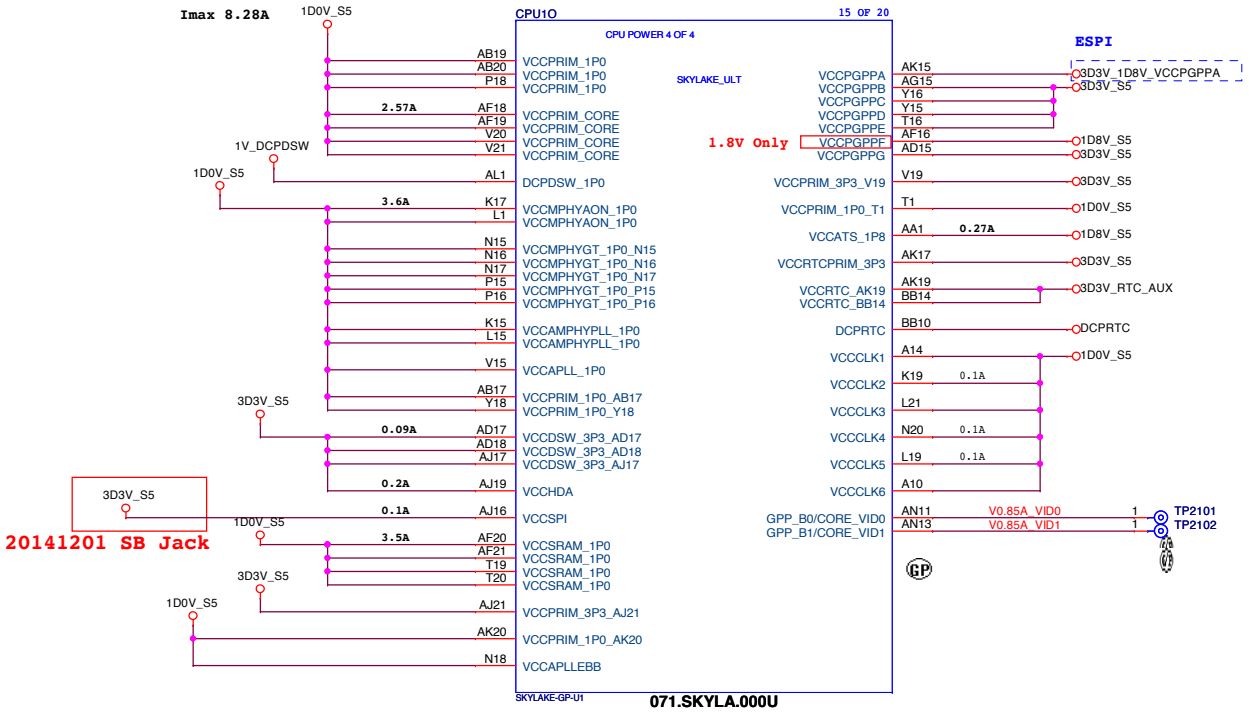
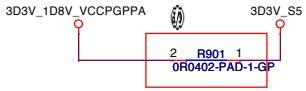
Main Func = PCH





20150415 -1

eSPI_508740:

Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_ 0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM L0ALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

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Title: CPU_(POWER1)

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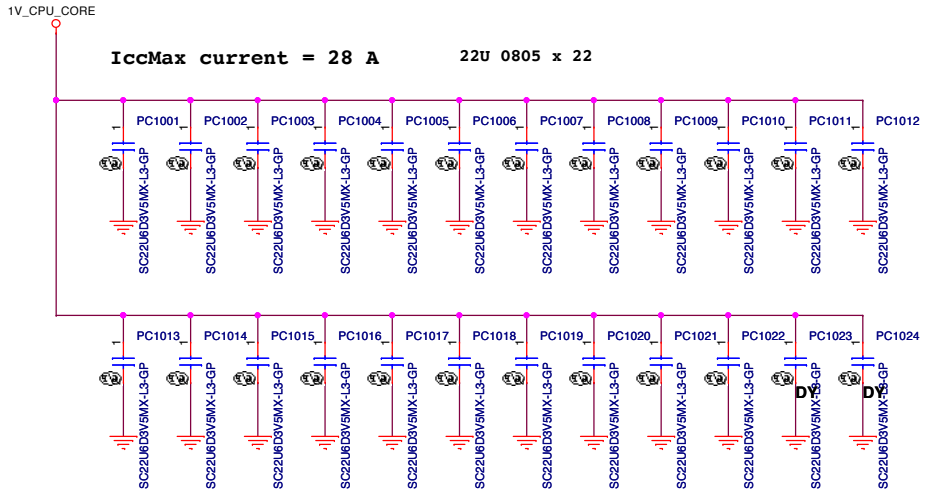
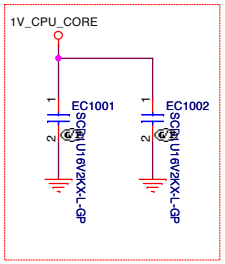
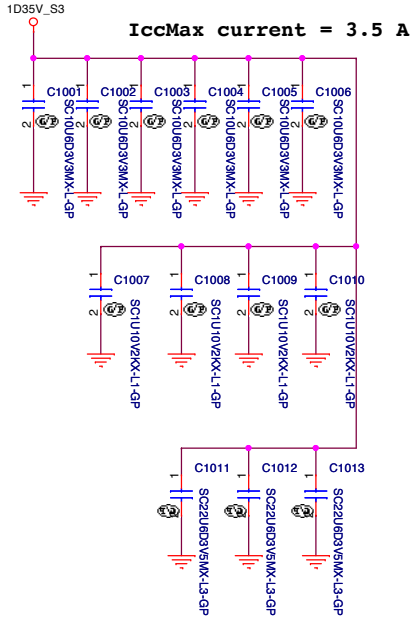
Main Func = CPU



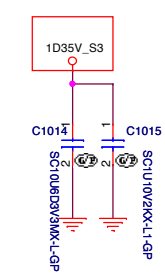


20150616 -1M



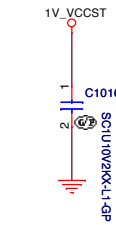
U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF

V_{DDQ}	2x 10 uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1 uF 0201 (Placeholder)		
		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible



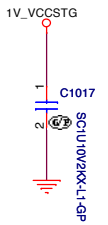
CLOSE CPU AM40

IccMax = 0.04 A



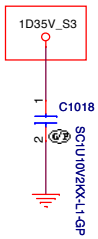
CLOSE CPU A18

IccMax = 0.04 A



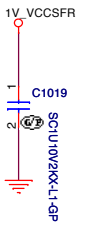
CLOSE CPU A22

IccMax = 0.26 A



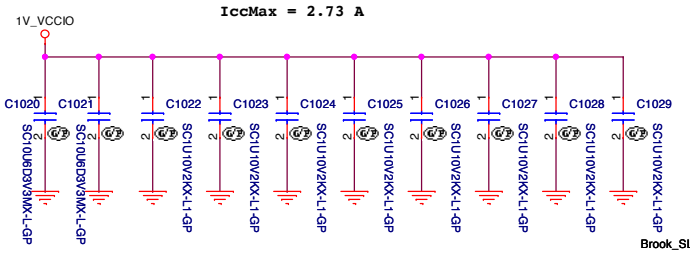
CLOSE CPU AL23

IccMax = 0.12 A



CLOSE CPU K20,K21

IccMax = 2.73 A



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Title	CPU_(Power CAP1)	
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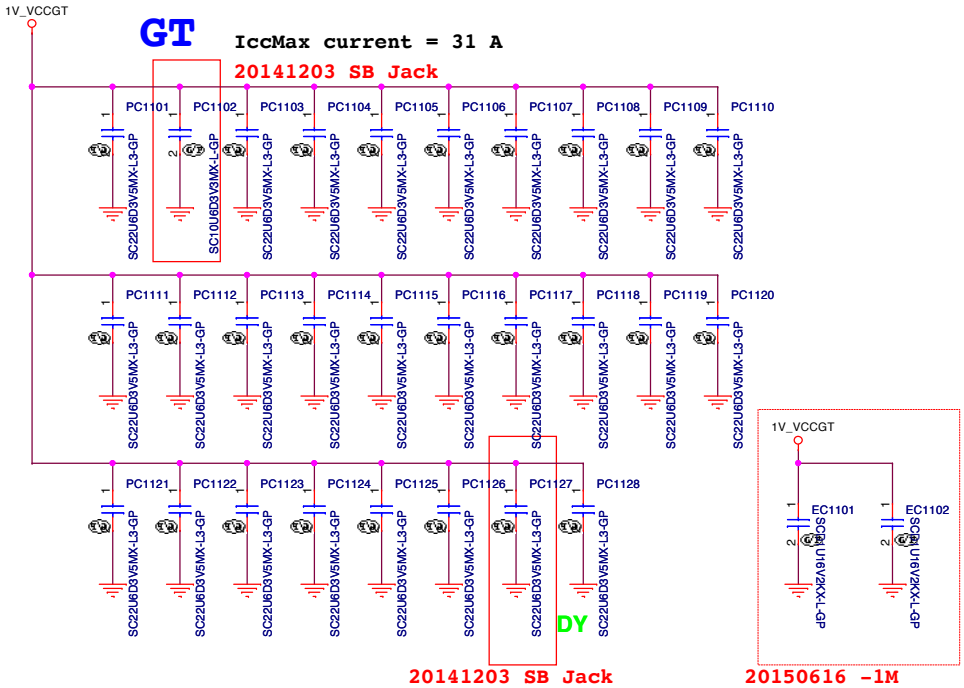
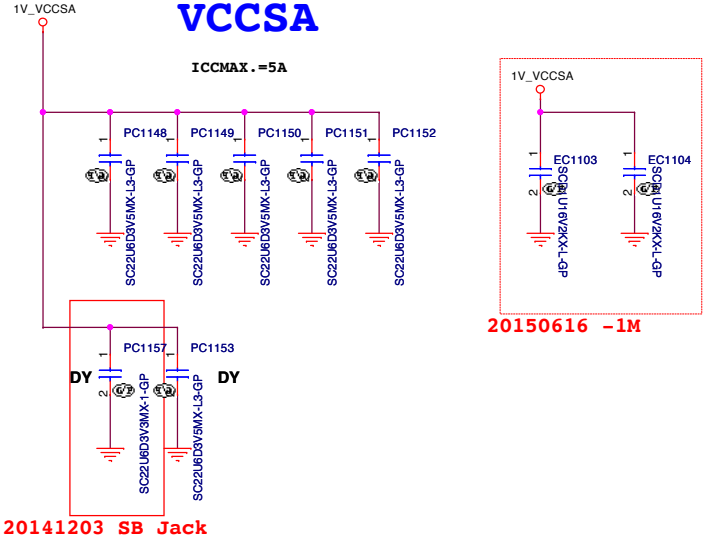
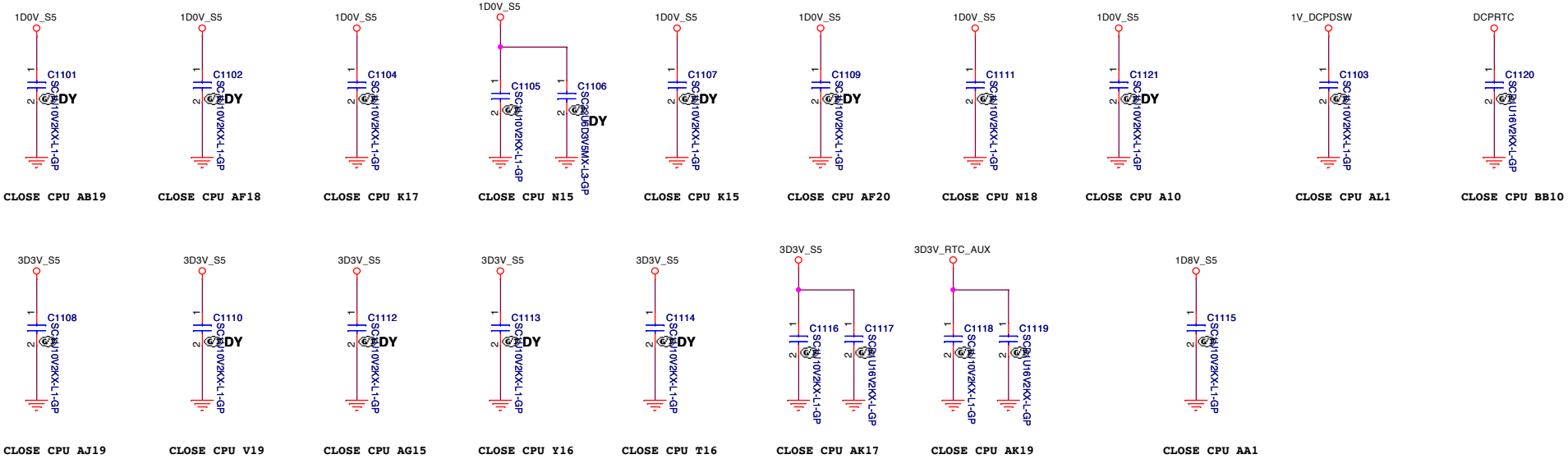
Main Func = CPU





U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF



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Title: CPU_(Power CAP2)

Size: A3 | Document Number: Brook_SLU | Rev: 1M

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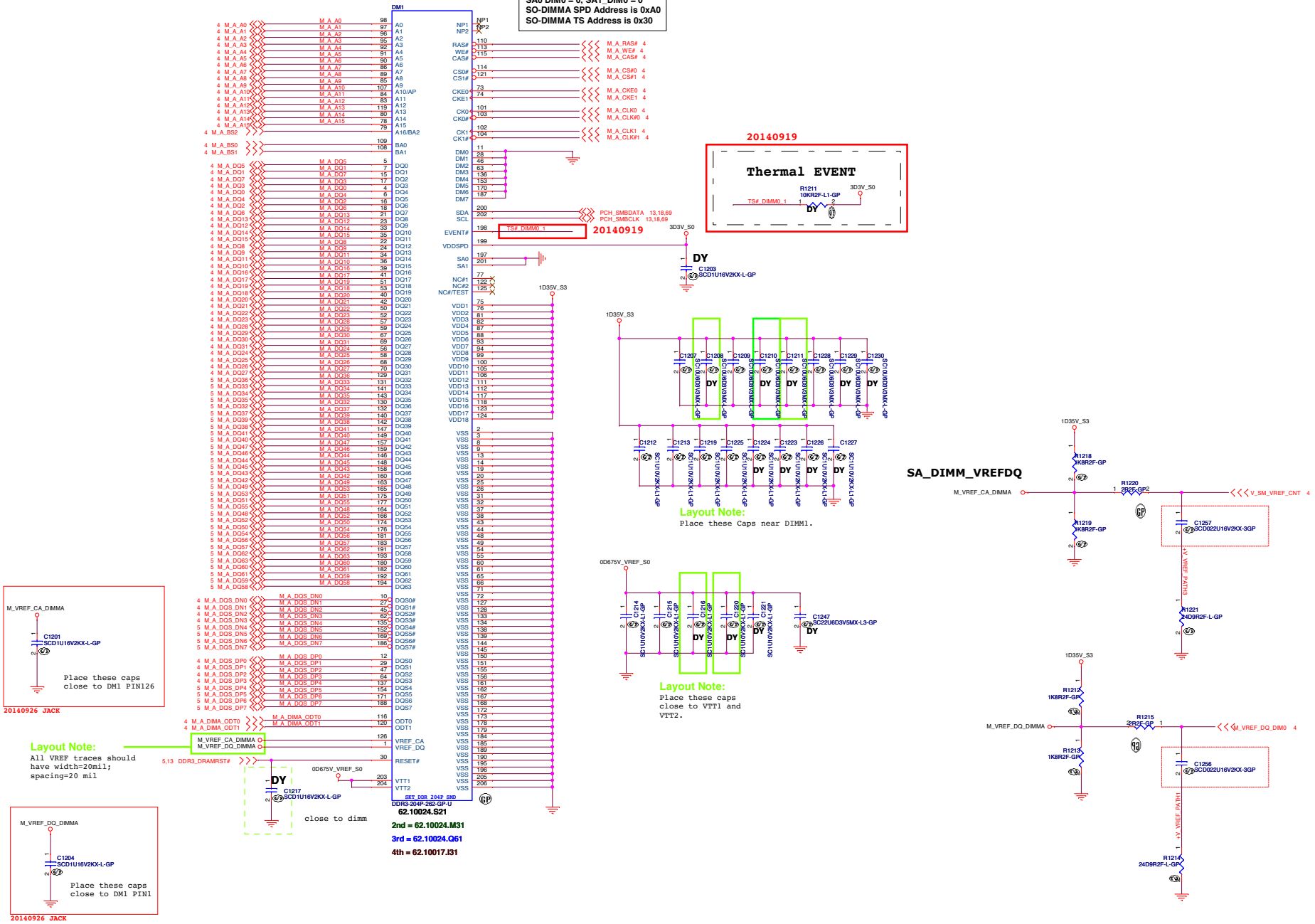
Main Func = DDR SODIMM

Note:
SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30



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Title: DDR3-SODIMM1

Size: A2 | Document Number: Brook_SLU | Rev: 1M

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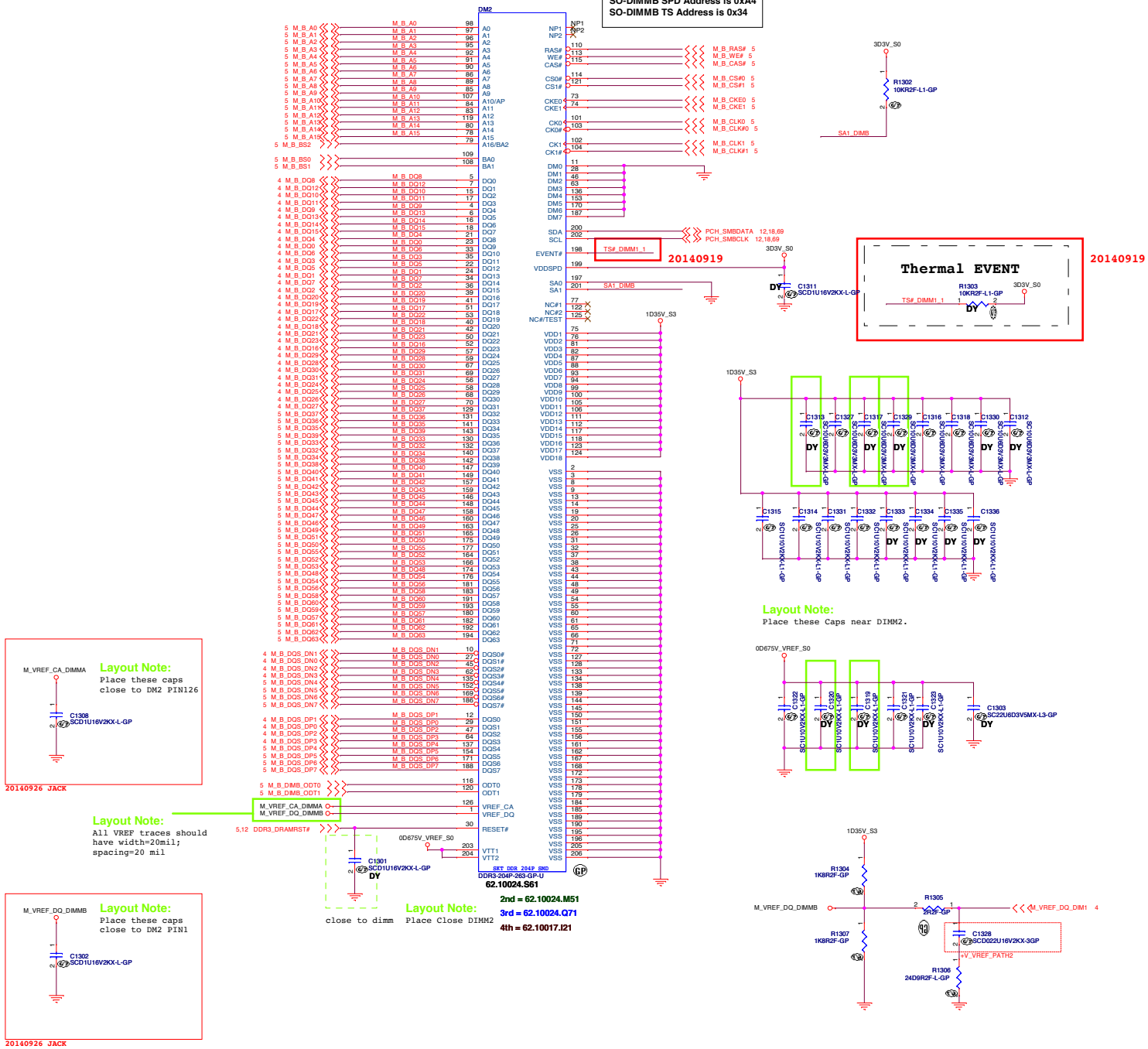
Main Func = DDR SODIMM

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34



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Title	***DDR3-SODIMM2***
Size A2 / Document Number	**Brook_SLU** / Rev **1M**
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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic	3D3V_S0 RN1401 SRN2K2J-5-GP HDMI_DATA_CPU 3,57 HDMI_CLK_CPU 3,57		3D3V_S5 R1441 10KR2J-3-GP DY SPI_SO_CPU 18	3D3V_S0 R1407 1KR2J-L2-GP DY GPP_B18/GSPI0_MOSI 6	3D3V_S0 R1408 1KR2J-L2-GP DY GPP_B22/GSPI1_MOSI 6		3D3V_S0 R1443 10KR2J-3-GP DY DDPD_CDA 3
High	Detected	Detected		Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected		Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic	3D3V_S0 R1415 1KR2J-L2-GP DY HDA_SPKR 17,27	3D3V_S5 R1435 10KR2J-3-GP DY SPI_SI_CPU 18	3D3V_S5 R1436 1KR2F-L1-GP SPI_WP_ROM_R 25	3D3V_S5 R1437 1KR2F-L1-GP SPI_HOLD_ROM_R 25	3D3V_S5 R1438 10KR2J-3-GP DY GPP_C2/SMBALERT# 18	3D3V_S5 R1439 10KR2J-3-GP DY GPP_C5/SML0ALERT# 18	3D3V_S5 R1440 150KR2J-GP DY 20150112 SC Jack GPP_B23/SML1ALERT# 18
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

<Core Design>

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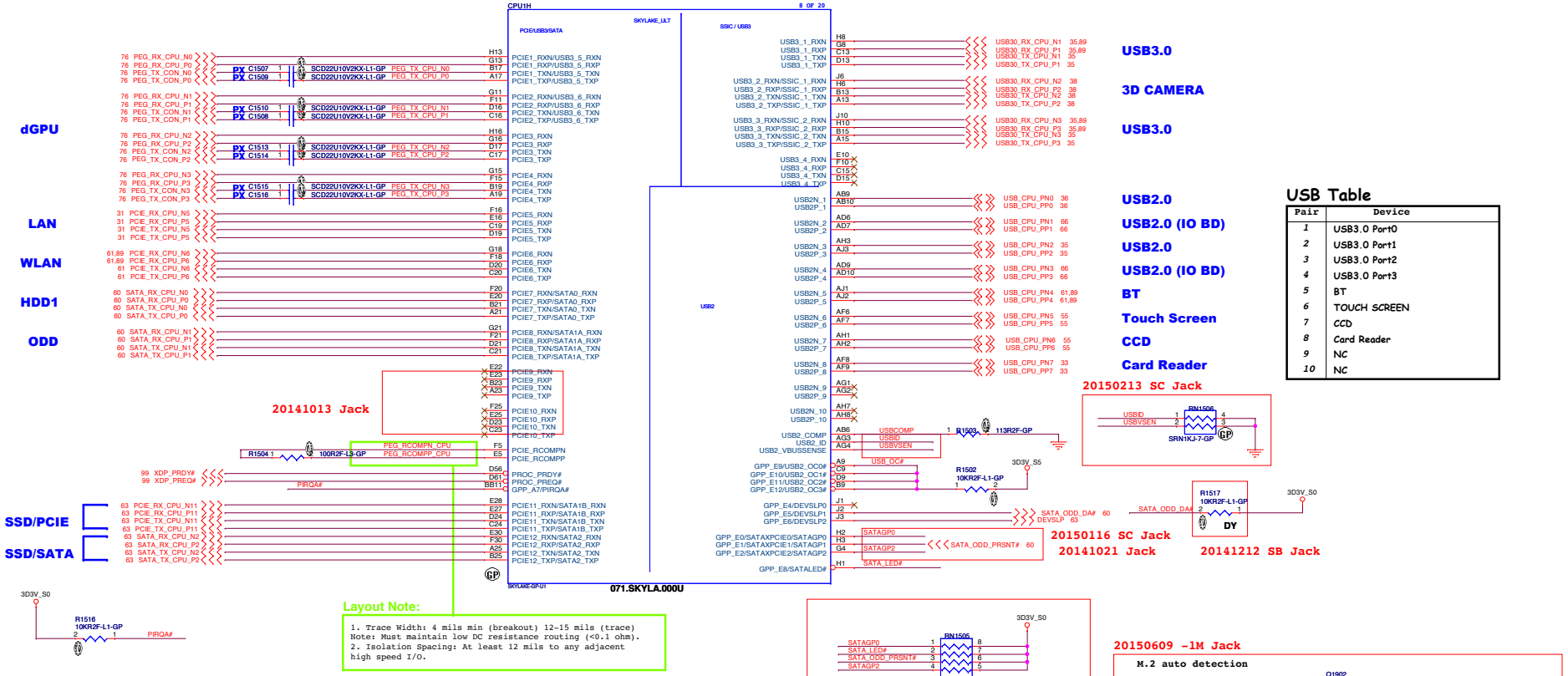
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)_SODIMM _SODIMM4

Size: A2 | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 06, 2015 | Sheet 14 of 105

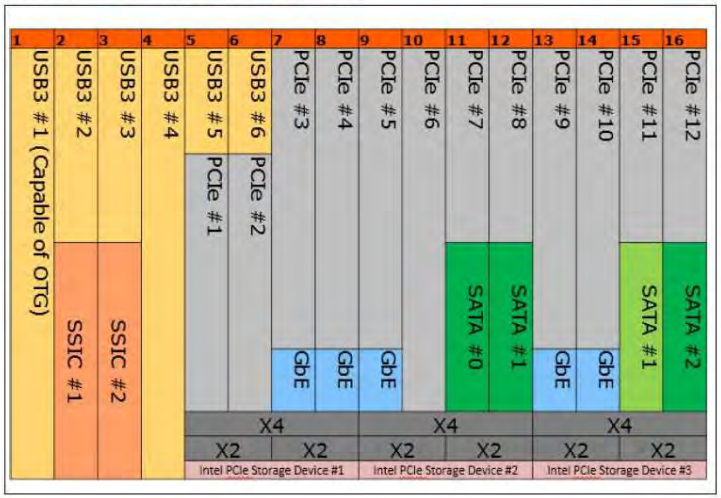
Main Func = PCH



USB Table

Pair	Device
1	USB3.0 Port0
2	USB3.0 Port1
3	USB3.0 Port2
4	USB3.0 Port3
5	BT
6	TOUCH SCREEN
7	CCD
8	Card Reader
9	NC
10	NC

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)



Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

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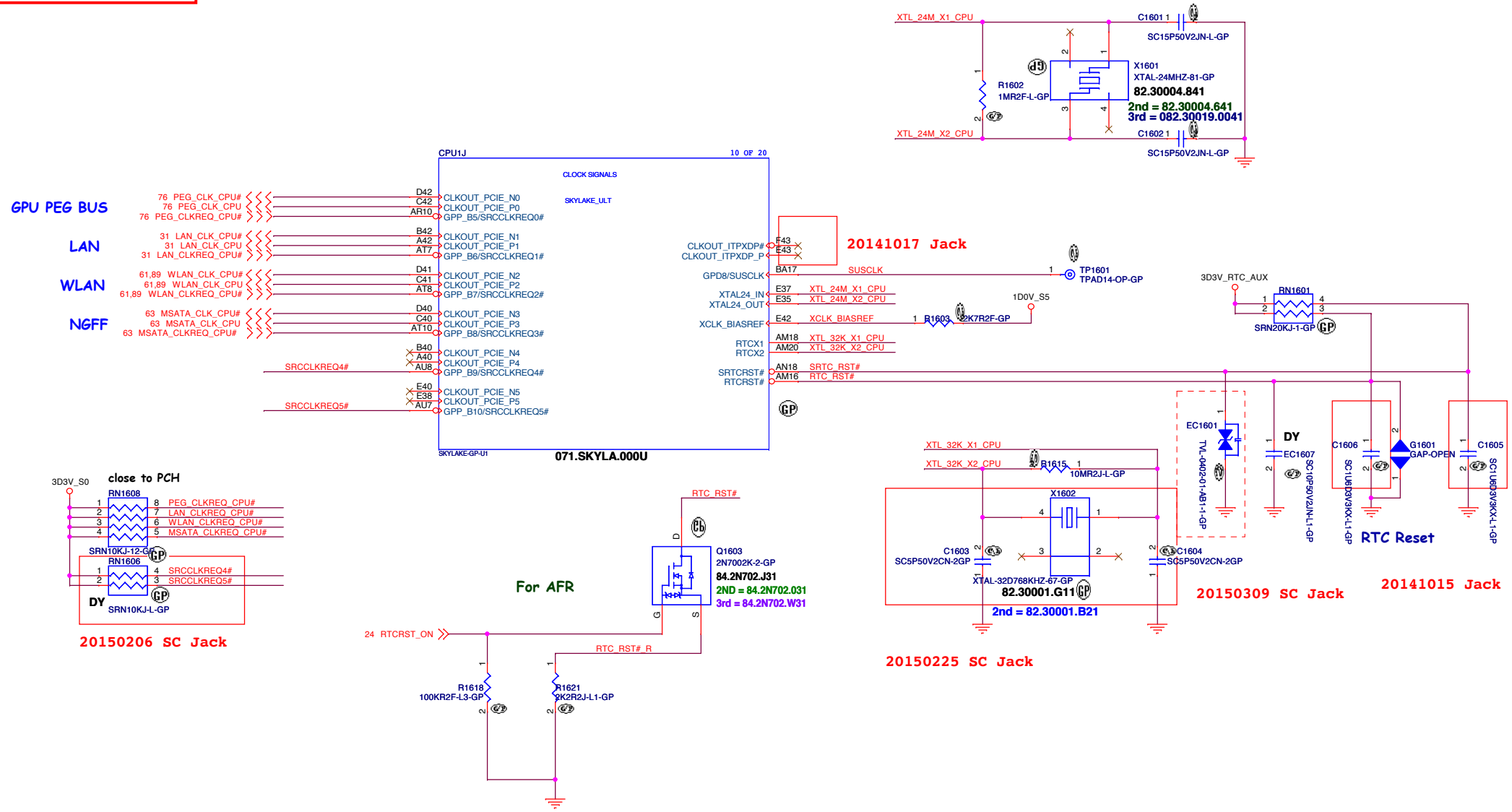
Title: CPU_(PCIE/SATA/USB)

Size: A2 | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 06, 2015 | Sheet 15 of 105

Main Func = PCH



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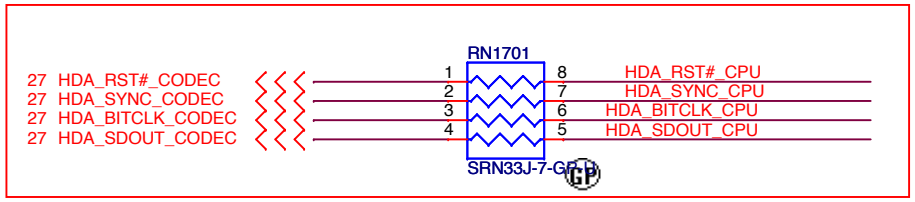
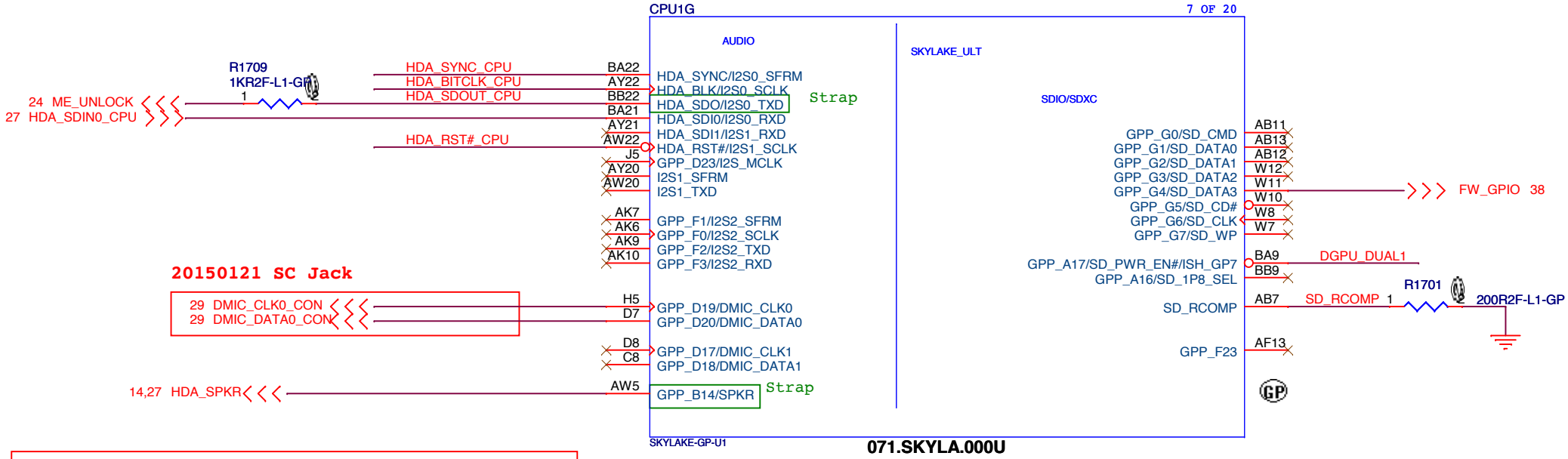
Title	MCP_CLOCK	
Size A3	Document Number Brook_SLU	Rev 1M
Date: Monday, July 06, 2015	Sheet 16 of 105	

Main Func = PCH

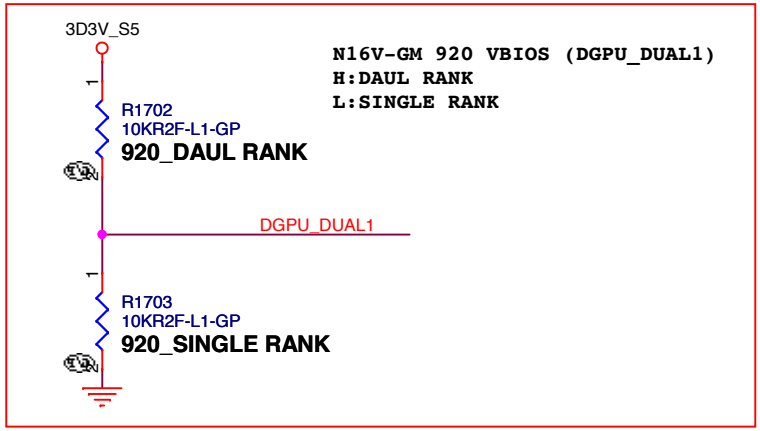


20150226 SC Jack



20150121 SC Jack

14,27 HDA_SPKR



20150202 SC Jack

<Core Design>

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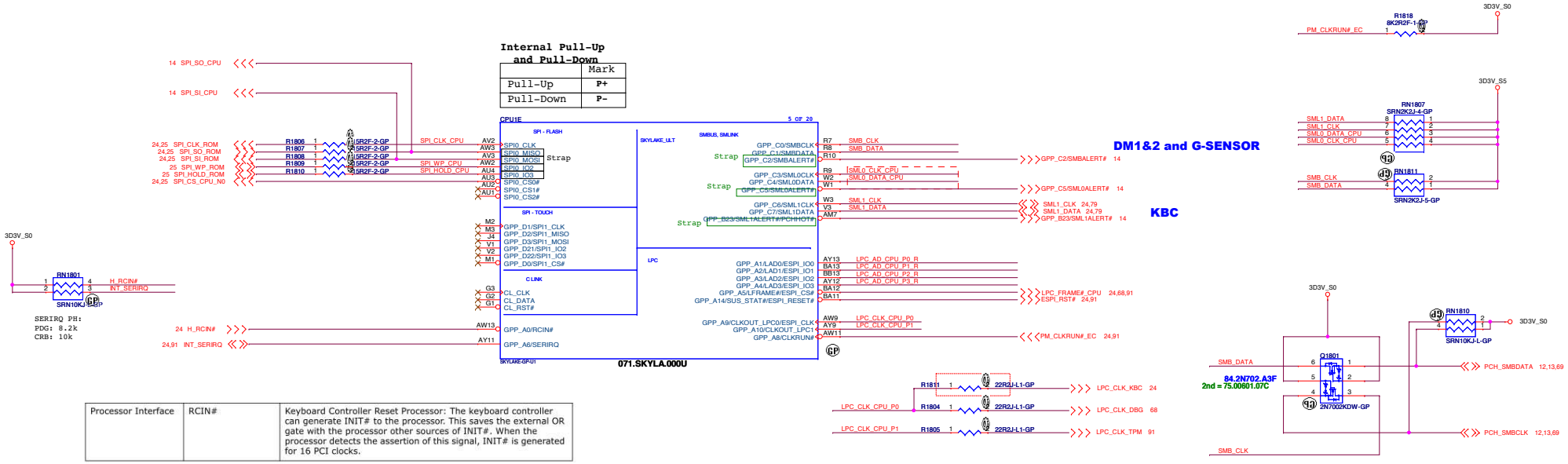
Title	CPU_(AUDIO/SDIO/SDXC)		
Size A4	Document Number Brook_SLU		Rev 1M
Date: Monday, July 06, 2015		Sheet 17 of 105	

Main Func = PCH

Internal Pull-Up and Pull-Down

	Mark
Pull-Up	P+
Pull-Down	P-



Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.

20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.

20150414 -1

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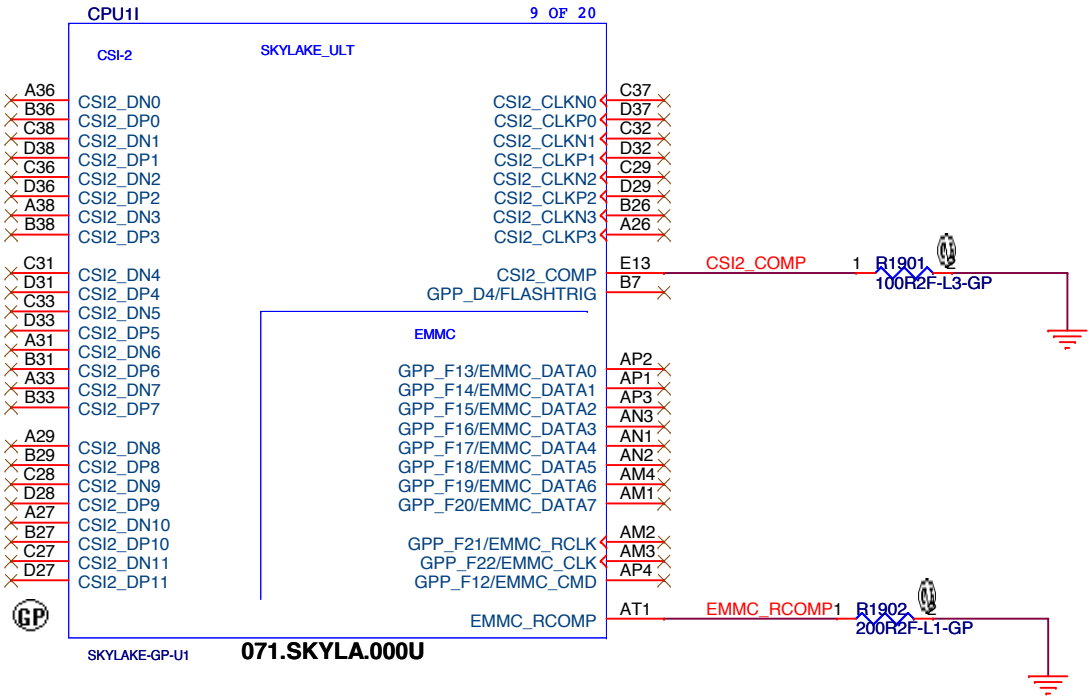
Title: LPC,SPI,SMBUS,CLINK

Size: A2 | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 06, 2015 | Sheet 18 of 105

Main Func = PCH



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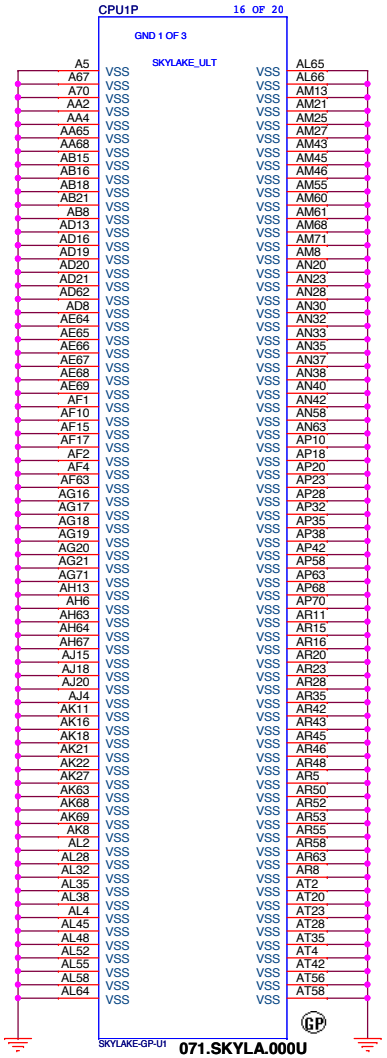
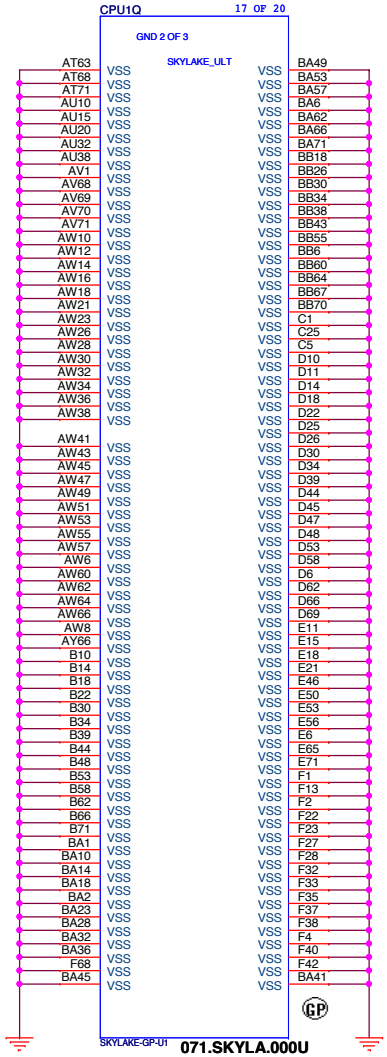
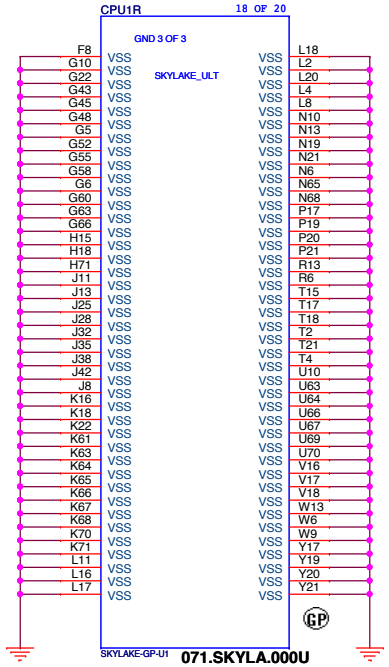
Title	***CPU_(CS-2/EMMC)***	
Size A4	Document Number **Brook_SLU**	Rev **1M**
Date: Monday, July 06, 2015	Sheet 19 of 105	

Main Func = PCH







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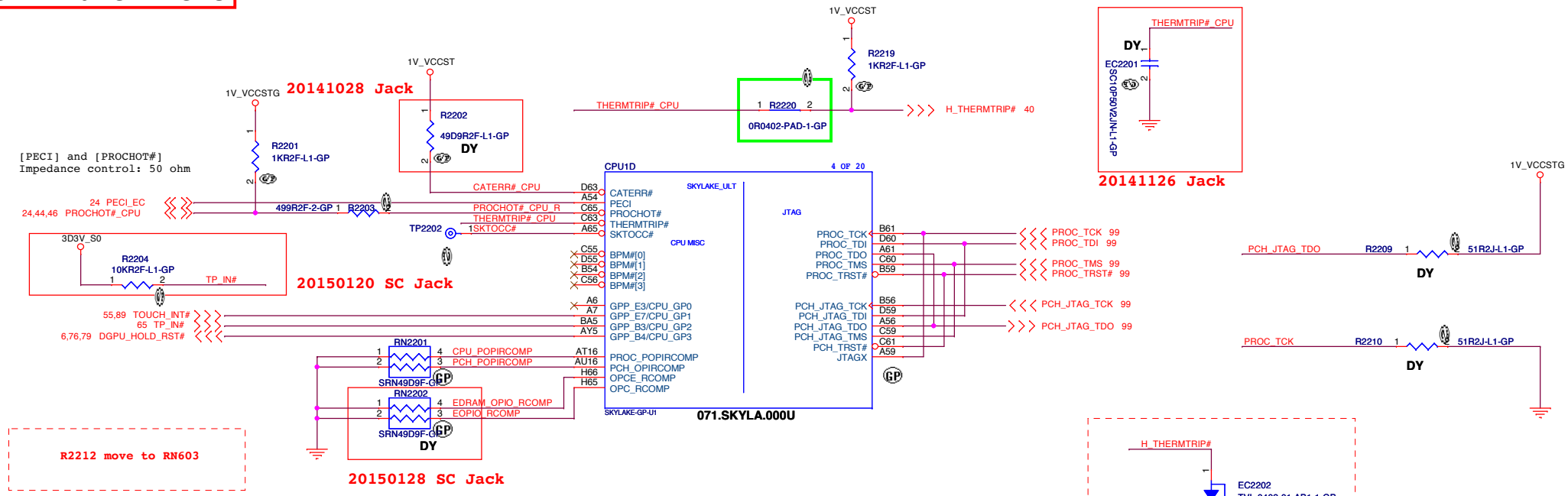
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

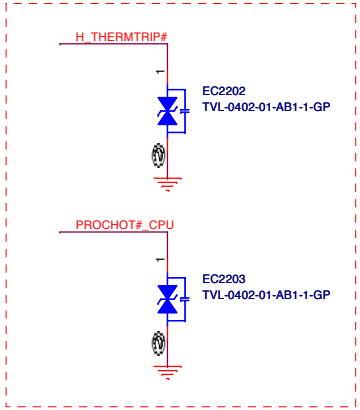
Title: ***CPU_(VSS)***

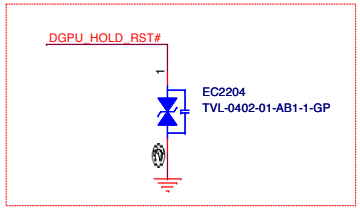
Size	Document Number	Rev
A3	Brook_SLU	1M

Date: Monday, July 06, 2015 Sheet 21 of 105

Main Func = CPU







20150325 SC

PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

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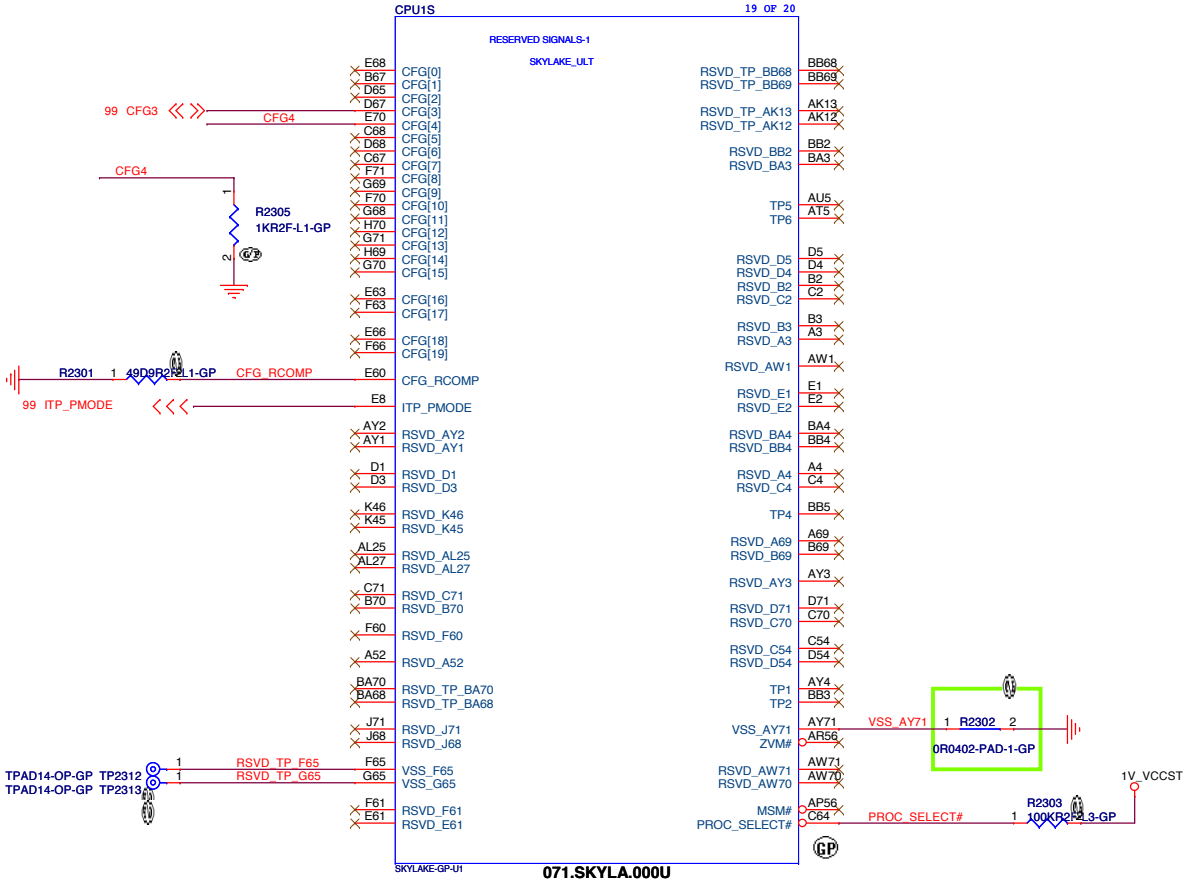
Title: **CPU_(JTAG/CPU SIDE BAND)**

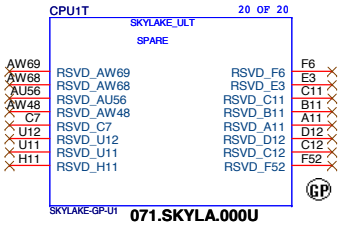
Size: A3 | Document Number: **Brook_SLU** | Rev: **1M**

Date: Monday, July 06, 2015 | Sheet 22 of 105

Main Func = CPU

CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.





PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines

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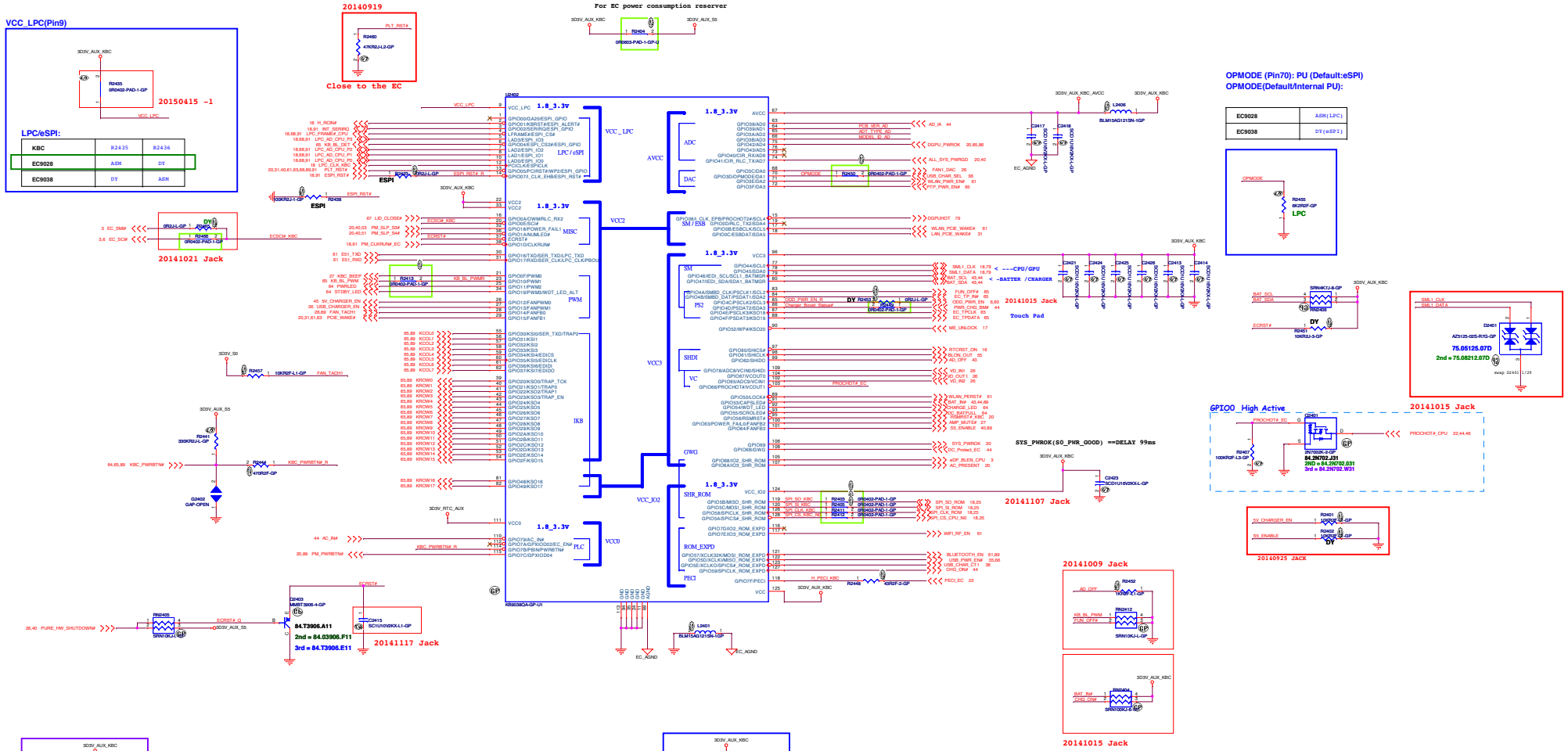
Title: ***CPU_RESERVED,CFG***

Size: A3 | Document Number: **Brook_SLU** | Rev: **1M**

Date: Monday, July 06, 2015 | Sheet 23 of 105

SSID = KBC



EC9028	ASM(LPC)
EC9038	DY(eSPI)

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
Brook_H_UMA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
Brook_H_DIS	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
Brook_B_UMA	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
Brook_B_DIS	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Brook_SL_UMA	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Brook_SL_DIS	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Min Voltage	KBC Firmware Setting	
3A	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
4B	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
5C	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
6	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.604 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.382 V	1.374 V	>= 1.281 V	< 1.604 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.046 V	1.062 V	>= 0.924 V	< 1.126 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Min Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	3.000 V			< 3.150 V
35W	10.0 K	100.0 K	0.385 V	0.385 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.750 V	0.769 V	>= 0.425 V	< 0.694 V
120W	33.0 K	100.0 K	0.917 V	0.931 V	>= 0.694 V	< 0.931 V
135W	47.0 K	100.0 K	1.050 V	1.070 V	>= 0.931 V	< 1.177 V
150W	64.9 K	100.0 K	1.289 V	1.319 V	>= 1.177 V	< 1.389 V
Reserved	76.8 K	100.0 K	1.482 V	1.492 V	>= 1.389 V	< 1.642 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.642 V	< 1.642 V

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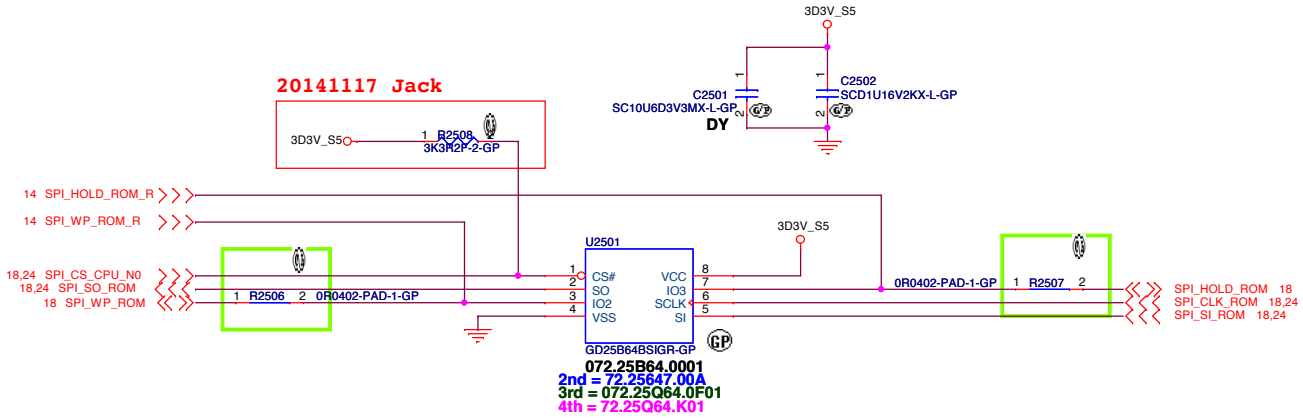
EC CONTROLLER

Size: A1 | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 08, 2013 | Sheet 24 of 105

Main Func = SPI Flash



SPI FLASH ROM (8M byte) for PCH

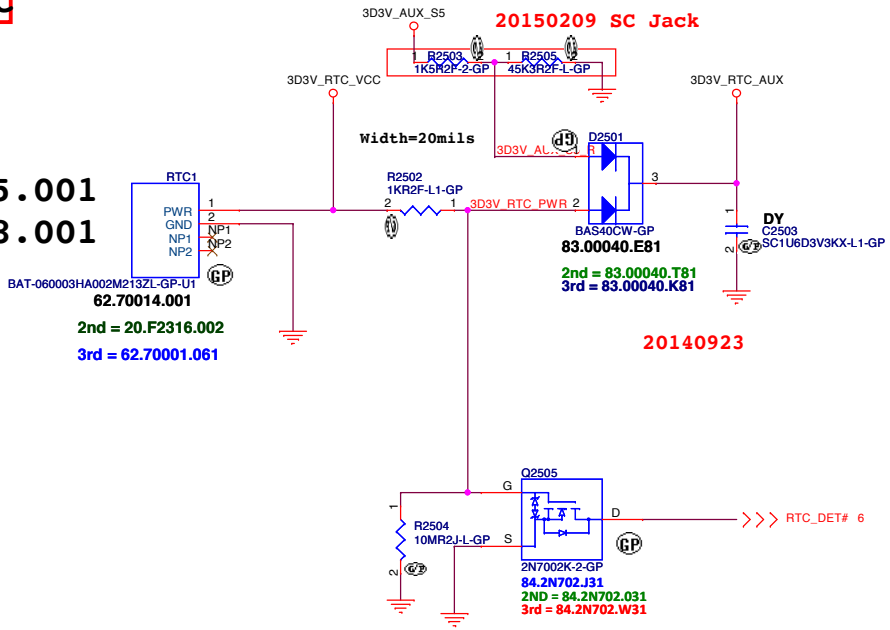
SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)

1st=072.25B64.0001(Gigadevice GD25B64BSIGR)
2nd=72.25647.00A (MXIC MX25L6473EM2I)
3rd=072.25Q64.0F01 (MICRON N25Q064A13ESED0F)
4rd=72.25Q64.K01 (WINBOND W25Q64FVSSIQ)

Main Func = RTC

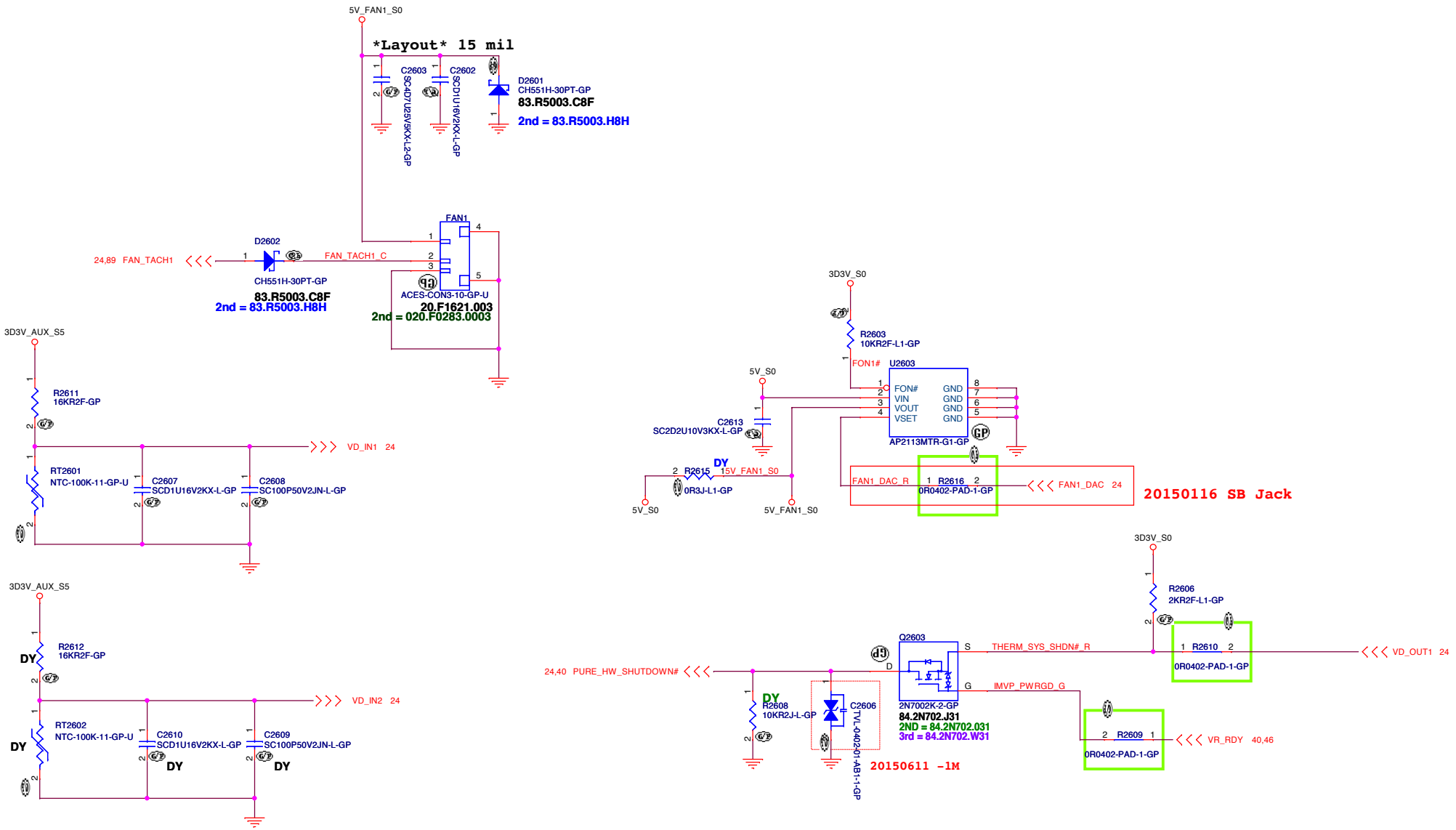
RTC BATTERY
1st= 23.22065.001
2nd= 23.20068.001



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Flash(KBC+PCH)/RTC***	
Size A3	Document Number **Brook_SLU**	Rev **1M**
Date: Monday, July 06, 2015	Sheet 25 of 105	

Main Func = Thermal Sensor



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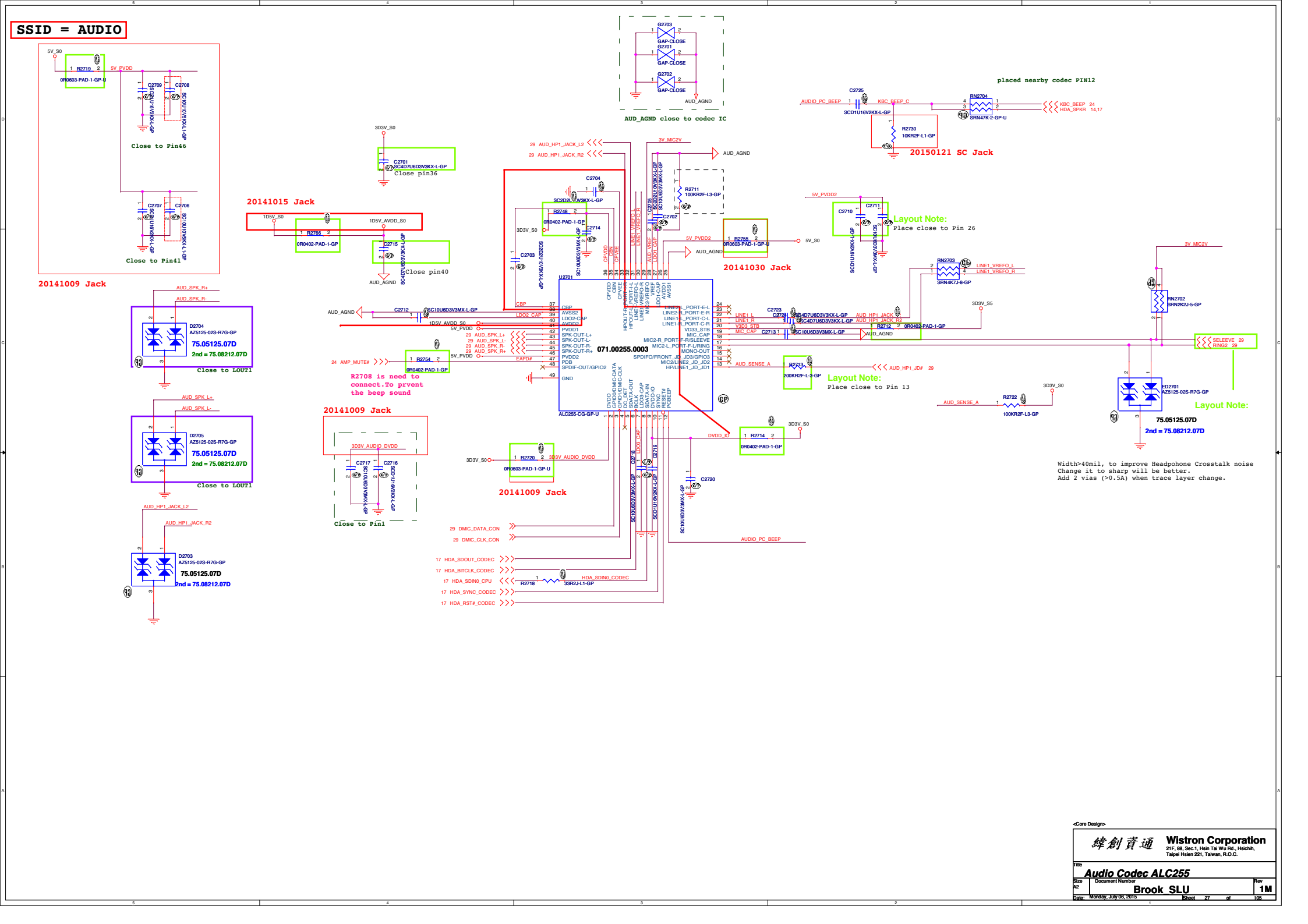
Title	***G788P81/Fan Controllor P2793***	
Size A3	Document Number **Brook_SLU**	Rev **1M**
Date: Monday, July 06, 2015	Sheet 26 of 105	


SSID = AUDIO
20141009 Jack
Close to Pin46
Close to Pin41
20141015 Jack
Close pin36
Close pin40
AUD_AGND close to codec IC
placed nearby codec PIN12
20150121 SC Jack
20141030 Jack
Layout Note:
Place close to Pin 26
Place close to Pin 13
R2708 is need to connect.To prvent the beep sound
071.00255.0003
ALC255-CG-GP-U
Close to LOUT1
Close to Pin1
75.05125.07D
2nd = 75.08212.07D
Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.
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Audio Codec ALC255
Brook_SLU
1M
Monday, July 06, 2015
Sheet 27 of 105

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Taipei Hsien 221, Taiwan, R.O.C.

Title
Audio AMP_1001

Size	Document Number	Rev
A4	**Brook_SLU**	**1M**

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SSID = AUDIO

Speaker

27 AUD_SPK_L- — R2914 0R0603-PAD-1-GP-U — AUD_SPK1_L- CON
27 AUD_SPK_L+ — R2915 0R0603-PAD-1-GP-U — AUD_SPK1_L+ CON
27 AUD_SPK_R- — R2916 0R0603-PAD-1-GP-U — AUD_SPK1_R- CON
27 AUD_SPK_R+ — R2917 0R0603-PAD-1-GP-U — AUD_SPK1_R+ CON

20150609 -1M

EC2901 SC22P50V2JN-L-GP DY
EC2902 SC22P50V2JN-L-GP DY
EC2915 SC22P50V2JN-L-GP DY
EC2920 SC22P50V2JN-L-GP DY

SPK1 — ES-CON4-17-GP-U
20.F1621.004
2nd = 020.F0155.0004

Layout Note:
Trace width=40mil

AUD_SPK1_L- CON — AUD_SPK1_L- CON 89
AUD_SPK1_L+ CON — AUD_SPK1_L+ CON 89
AUD_SPK1_R- CON — AUD_SPK1_R- CON 89
AUD_SPK1_R+ CON — AUD_SPK1_R+ CON 89

AFTP TESTPOINT

AUD_SPK1_L- CON — ED2901 AZ5125-02S-R7G-GP 2nd = 75.08212.07D DY
AUD_SPK1_L+ CON
AUD_SPK1_R- CON — ED2902 AZ5125-02S-R7G-GP 2nd = 75.08212.07D DY
AUD_SPK1_R+ CON

20141016 Jack

Combo Jack

R2910 0R0402-PAD-1-GP DY
AUD_HP1_JD# R — Q2901 2N7002K-2-GP — AUD_HP1_JD# 27
84.2N702.J31
2nd = 84.2N702.031
3rd = 84.2N702.W31
C2902 SC10U6D3V3MX-L-GP DY
R2901 100KR2J-4-GP DY
AUD_AGND

3D3V_S0
R2905 10KR2J-L-GP DY
AUD_HP1_JD# TYPE — AUD_HP1_JD#_TYPE 89
R2906 0R0402-PAD-1-GP
AUD_AGND

0527_SB

27 RING2 — ER2913 — R2920 0R0402-PAD-1-GP — 57D6R2F-GP — RING2_R
27 AUD_HP1_JACK_L2 — AUD_HP1_JACK_L1
27 AUD_HP1_JACK_R2 — ER2912 — R2921 0R0402-PAD-1-GP — 57D6R2F-GP
27 SELEEVE — AUD_HP1_JD# TYPE, AUD_HP1_JD# R, AUD_HP1_JACK_R1, SELEEVE_R

AUD1 audio(IP/NK comb) AUDIO-JK506-GP-U
022.10002.0951
AUD_AGND

EC2921 SC22P50V2JN-L-GP DY
EC2922 SC22P50V2JN-L-GP DY
EC2912 SC22P50V2JN-L-GP DY
EC2913 SC22P50V2JN-L-GP DY
EC2914 SC22P50V2JN-L-GP DY

AUD_HP1_JD# R — AUD_HP1_JD#_R 89
AUD_HP1_JACK_R1 — AUD_HP1_JACK_R1 89
AUD_HP1_JACK_L1 — AUD_HP1_JACK_L1 89
RING2_R — RING2_R 89
SELEEVE_R — SELEEVE_R 89
AUD_HP1_JD# TYPE — AUD_HP1_JD#_TYPE 89

AFTP TESTPOINT

3D3V_S0
R2923 0R2J-L-GP DUAL
R2924 0R2J-L-GP SINGLE
MIC2_EN, DMIC_DATA_R
MIC2 ENHANCE, CS, GND, VDD, DATA, CLK — MICROPHONE-105-GP-U 082.40011.0001 — DMIC_DATA_CON_R, DMIC_CLK_CON_R — 3D3V_S0

20141208 SB Jack

MIC1 ENHANCE, CS, GND, VDD, DATA, CLK — MICROPHONE-105-GP-U 082.40011.0001 — DMIC_DATA_R1, DMIC_CLK_CON_R1 — 3D3V_S0

DUAL MIC=082.40011.0001

SINGALE MIC
=082.40006.0001 (1ST)
=082.40002.0031 (2ND)
=082.40011.0011 (3RD)

20150121 SC

R2261 0R2J-L-GP DY — DMIC_DATA0_CON 17
R2251 0R2J-L-GP DY — DMIC_CLK0_CON 17
R2091 0R2J-L-GP — DMIC_CLK_CON 27
R2911 0R2J-L-GP — DMIC_DATA_CON 27
R2912 0R2J-L-GP DUAL — DMIC_CLK_CON
DMIC_CLK_CON_R, DMIC_DATA_CON_R, DMIC_CLK_CON_R1
EC2903 SC4D7P50V2BN-GP DY
EC2904 SC4D7P50V2BN-GP DY
EC2905 SC4D7P50V2BN-GP DY

DMIC_DATA_R — R2919 0R2J-L-GP SINGLE

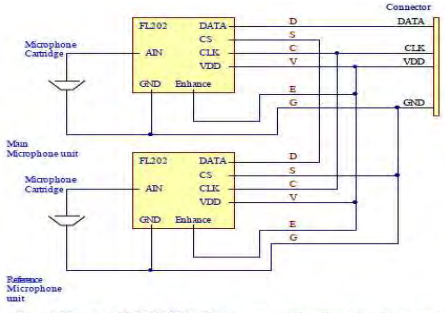

Figure 4 Schematic of NSM0410DT iSAM enhance array configuration (2 microphones array)

CLK_CON_MIC3
DATA_CON_MIC3
EC2908 SC4D7P50V2BN-GP DY
EC2907 SC4D7P50V2BN-GP DY

MIC3 PTWO-CON4-9-GP-U DY
3D3V_S0
CLK_CON_MIC3, DATA_CON_MIC3

R2271 0R2J-L-GP DY — DMIC_DATA0_CON 17
R2281 0R2J-L-GP DY — DMIC_CLK0_CON 17
R2181 0R2J-L-GP DY — DMIC_CLK_CON 27
R2922 0R2J-L-GP DY — DMIC_DATA_CON 27

20150121 SC

DMIC_DATA_R1 — R2913 0R2J-L-GP DUAL — DMIC_DATA_R
EC2906 SC4D7P50V2BN-GP DY

20141015 Jack

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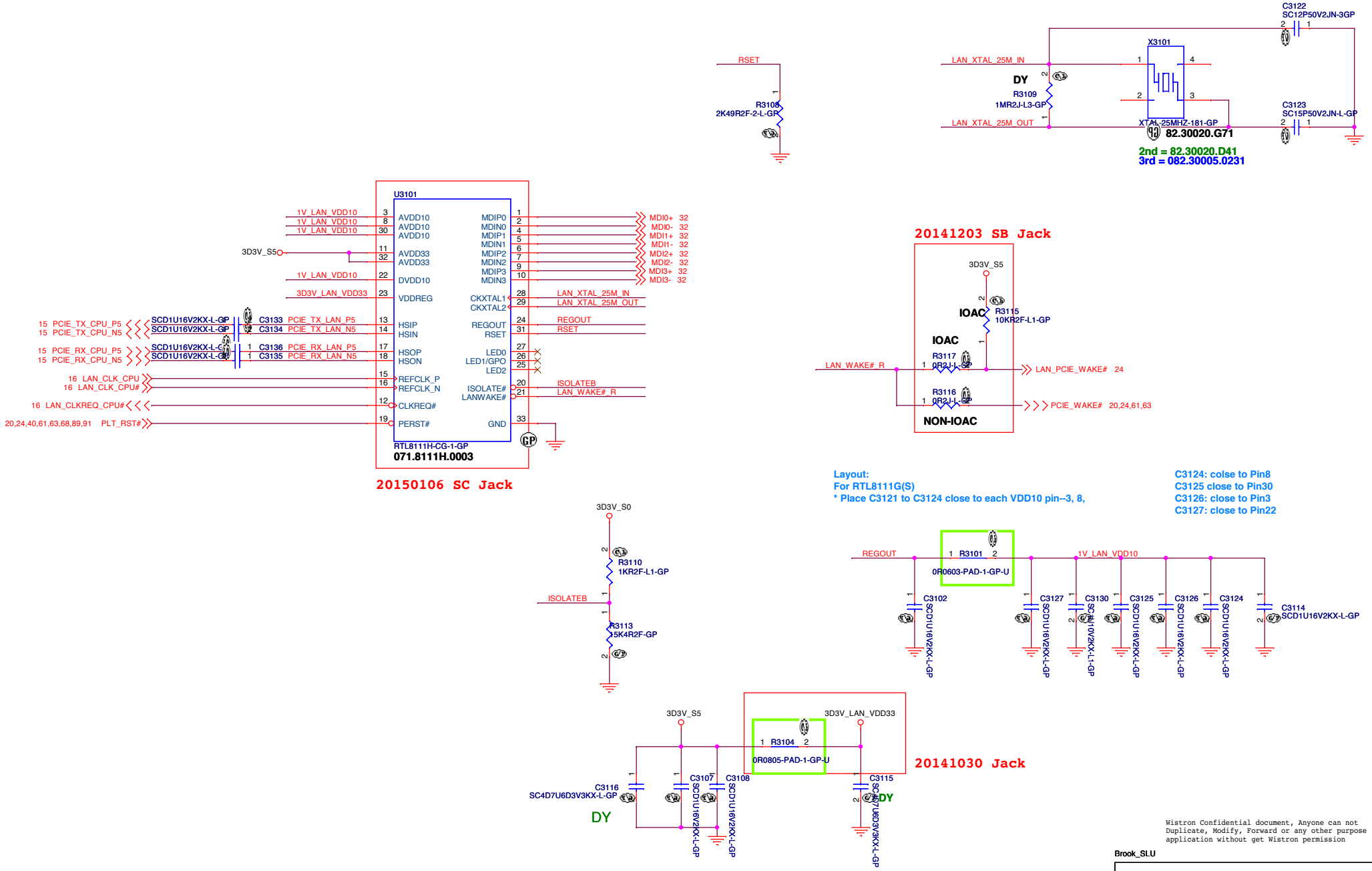
Title		
Size A	Document Number **Brook_SLU**	Rev **1M**
Date: Monday, July 06, 2015	Sheet 30 of 105	



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Size	Document Number	Rev
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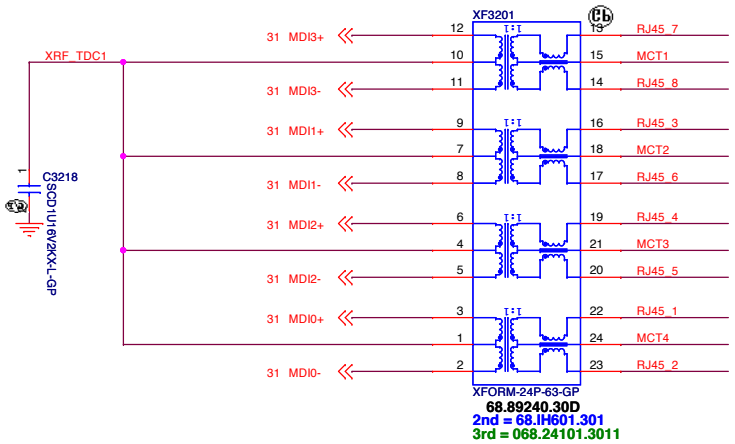
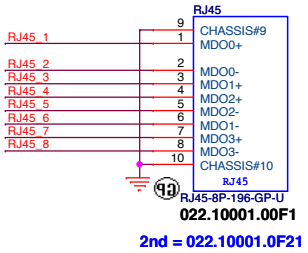
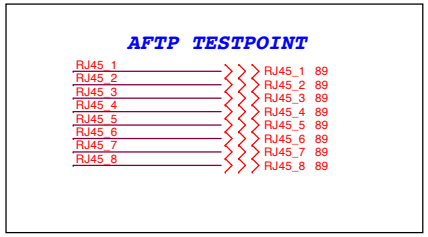
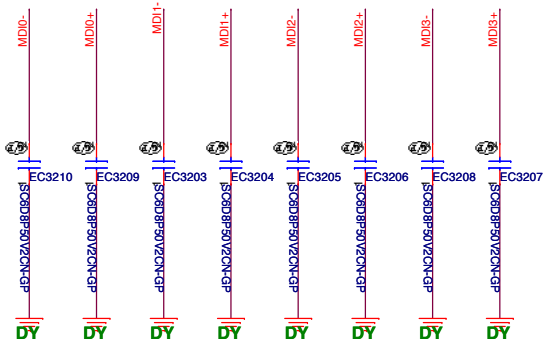
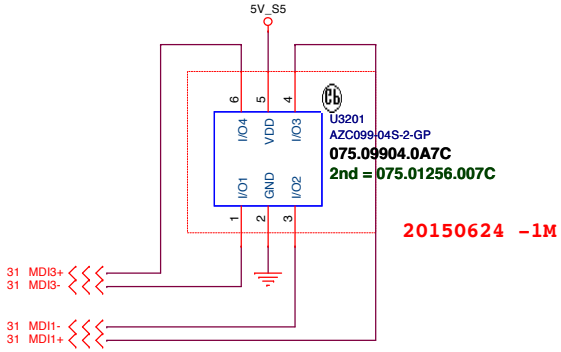
SSID = LAN

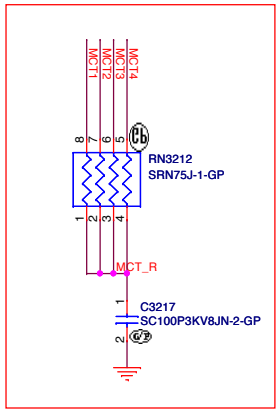


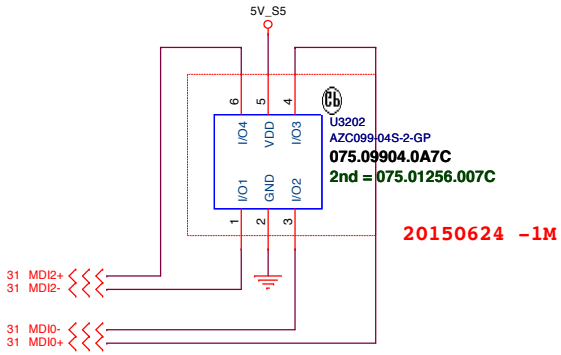












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Title: **(LAN+VGA) CONNECTOR**

Size	Document Number	Rev
A3	Brook_SLU	1M

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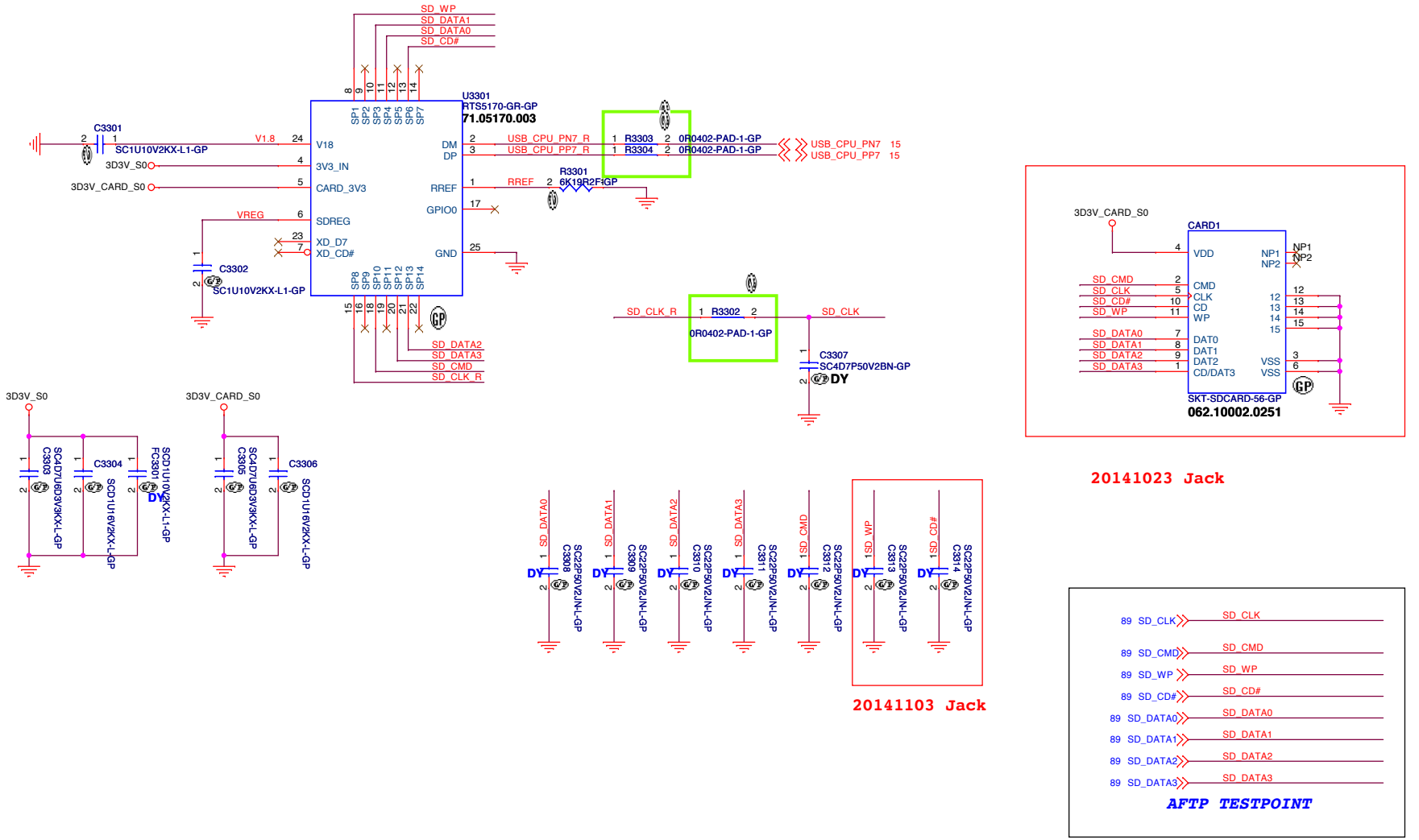

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Title: **Card Reader IC+Reader Conn**

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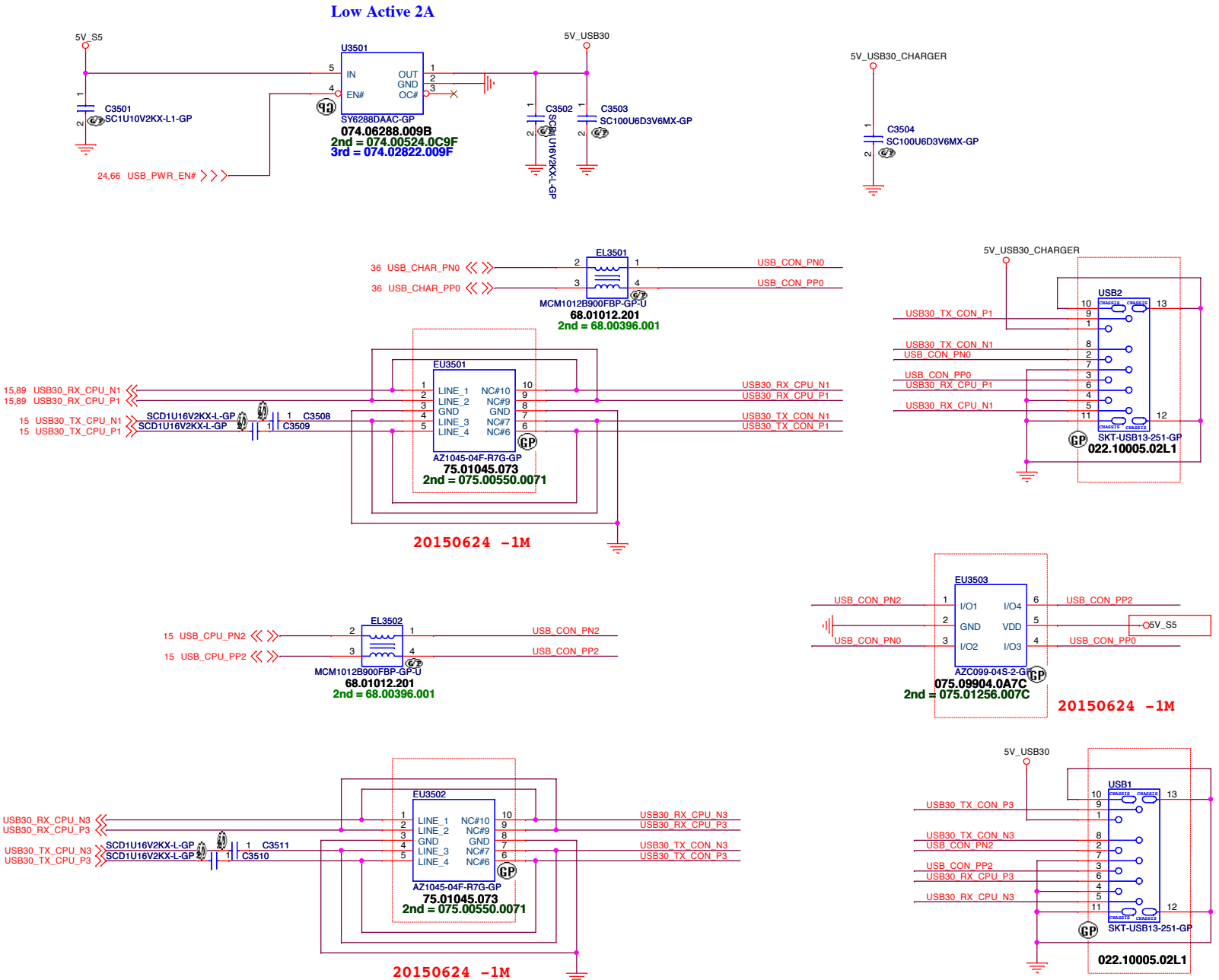
Title	USB2.0 CONN	
Size A3	Document Number Brook_SLU	Rev 1M
Date: Monday, July 06, 2015	Sheet 34 of 105	

USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



AFTP TESTPOINT

USB30_TX_CON_P1	USB30_TX_CON_P1 89
USB30_TX_CON_N1	USB30_TX_CON_N1 89
USB_CON_PN0	USB_CON_PN0 89
USB_CON_PP0	USB_CON_PP0 89
USB30_RX_CPU_P1	USB30_RX_CPU_P1 15,89
USB30_RX_CPU_N1	USB30_RX_CPU_N1 15,89
USB30_TX_CON_P3	USB30_TX_CON_P3 89
USB30_TX_CON_N3	USB30_TX_CON_N3 89
USB_CON_PN2	USB_CON_PN2 89
USB_CON_PP2	USB_CON_PP2 89
USB30_RX_CPU_P3	USB30_RX_CPU_P3 15,89
USB30_RX_CPU_N3	USB30_RX_CPU_N3 15,89

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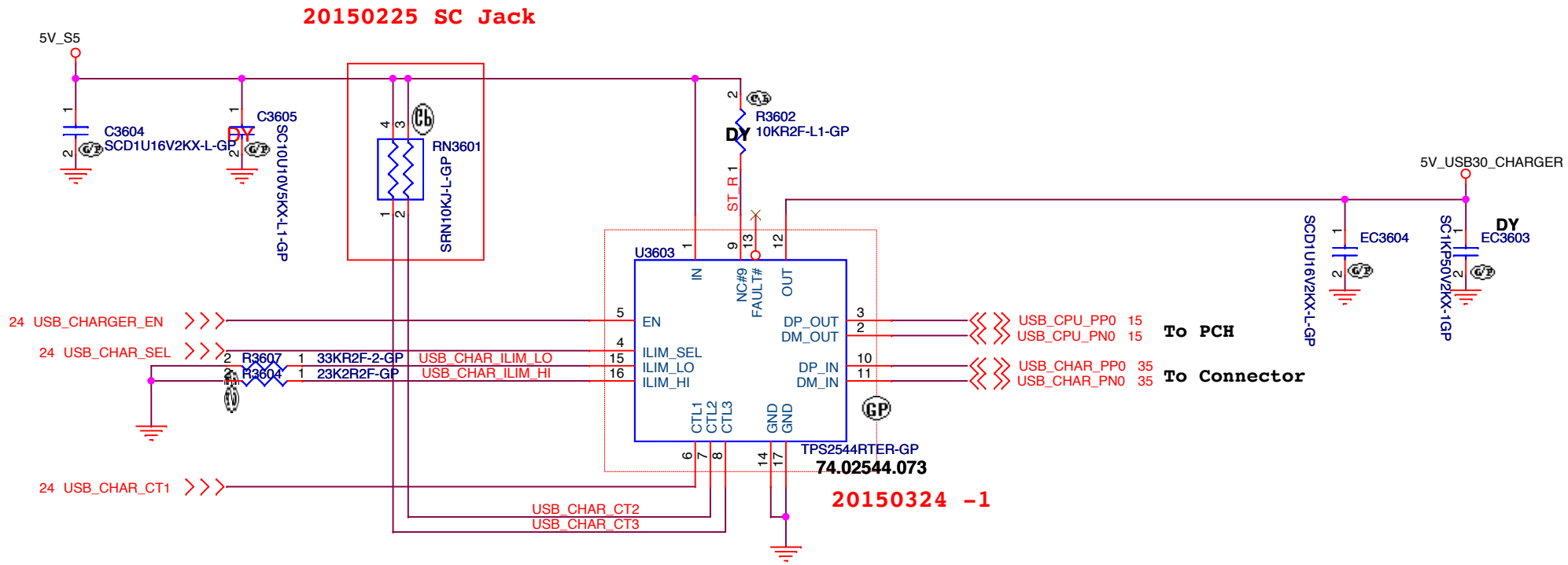
Title: USB3.0 CONN

Size: A3 | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 06, 2015 | Sheet 35 of 105



	Device Control Pins			
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
	0	1	1	X

3.Electrical Safety for USB3.0 Port

2.0 A <= Measurement value <= 2.2 A : Pass

1.9 A <= Measurement value < 2.0 A or 2.2 A < Measurement value <= 2.4 A : Marginal

If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port.

And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A – 2.4 A).

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Title: **USB CHARGER**

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Title ***Reserved***

Size	Document Number	Rev
A4	**Brook_SLU**	**1M**

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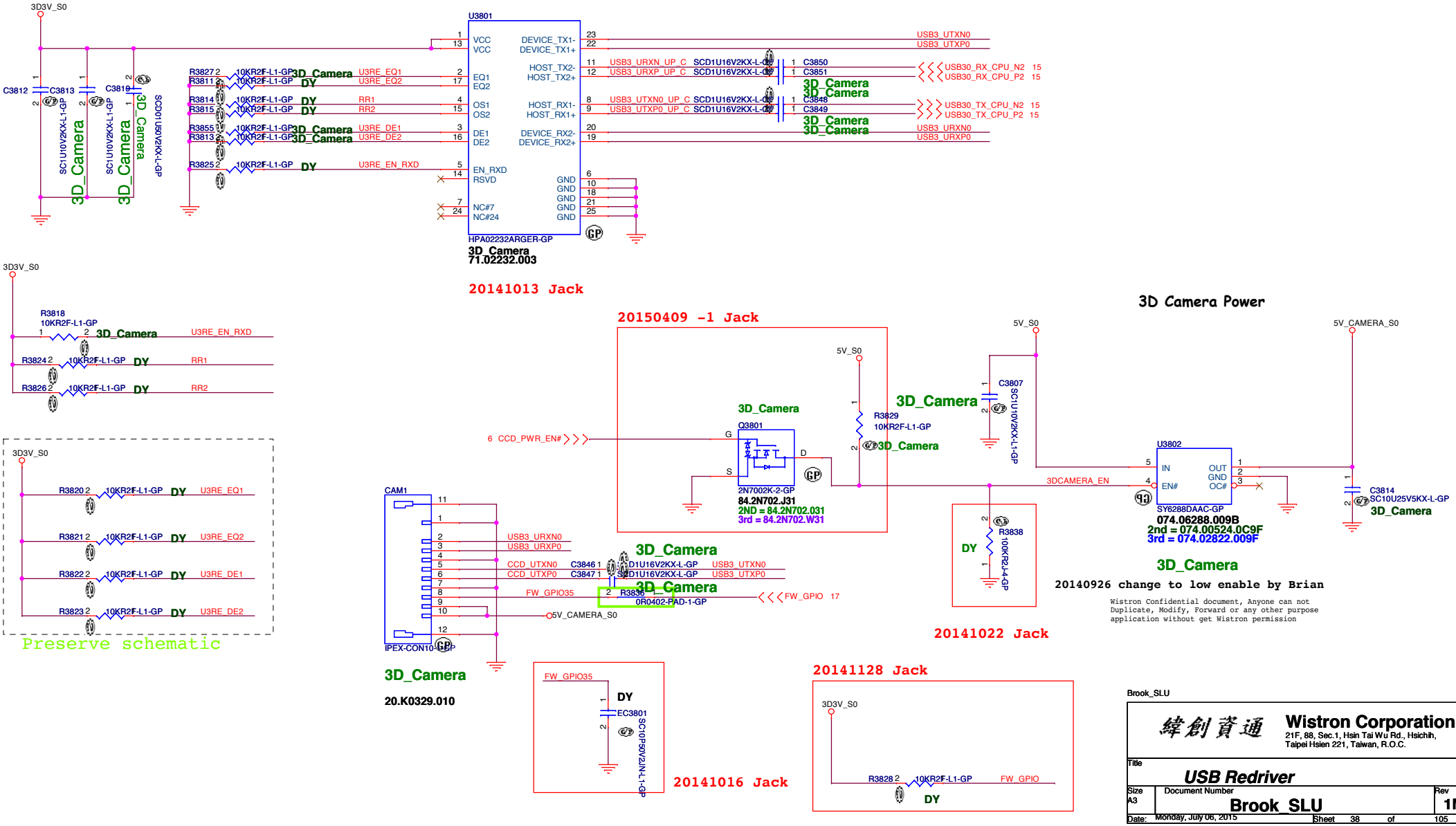
3D3V_S0
U3801
VCC
VCC
DEVICE_TX1-
DEVICE_TX1+
HOST_TX2-
HOST_TX2+
HOST_RX1-
HOST_RX1+
DEVICE_RX2-
DEVICE_RX2+
EQ1
EQ2
OS1
OS2
DE1
DE2
EN_RXD
RSVD
NC#7
NC#24
GND
HPA02232ARGER-GP
3D_Camera
71.02232.003
20141013 Jack
USB3_UTXN0
USB3_UTXP0
USB3_URXN0
USB3_URXP0
USB30_RX_CPU_N2
USB30_RX_CPU_P2
USB30_TX_CPU_N2
USB30_TX_CPU_P2
U3RE_EQ1
U3RE_EQ2
RR1
RR2
U3RE_DE1
U3RE_DE2
U3RE_EN_RXD
10KR2F-L1-GP
SCD1U16V2KX-L-GP
SC1U10V2KX-L1-GP
SCD01U50V2KX-L-GP
DY
3D Camera Power
20150409 -1 Jack
5V_S0
5V_CAMERA_S0
Q3801
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
R3829
C3807
U3802
IN
OUT
GND
EN#
OC#
SY6288DAAC-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
C3814
SC10U25V5KX-L-GP
3DCAMERA_EN
CCD_PWR_EN#
R3838
100KR2J-4-GP
20140926 change to low enable by Brian
20141022 Jack
CAM1
IPEX-CON10-GP
CCD_UTXN0
CCD_UTXP0
FW_GPIO35
FW_GPIO
5V_CAMERA_S0
0R0402-PAD-1-GP
20.K0329.010
EC3801
SC10P50V2JN-L-GP
20141016 Jack
20141128 Jack
R3828
Preserve schematic
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Title

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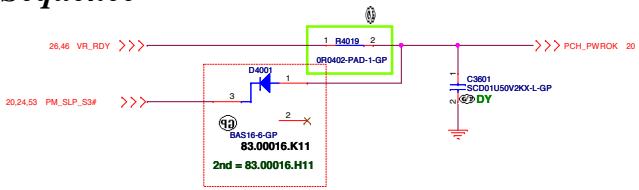
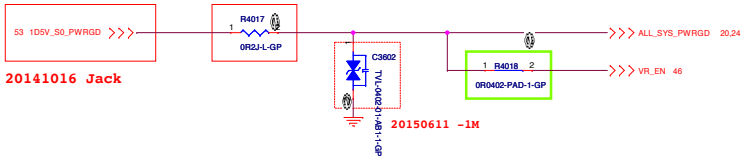
Power Sequence



20150629 -1M

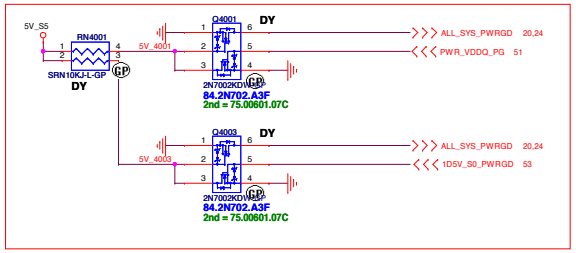
20150413 -1 Jack



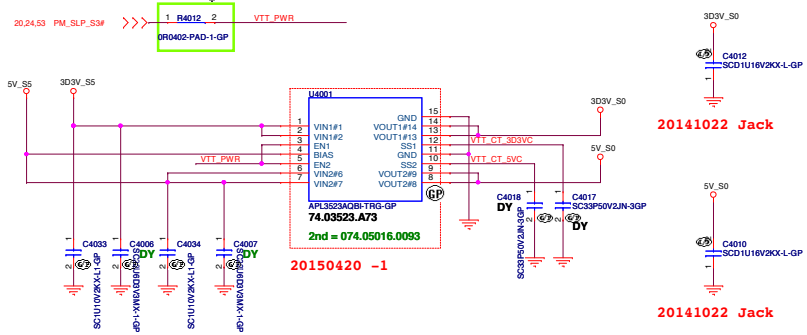
20141016 Jack

20150611 -1M

20150413 -1 Jack



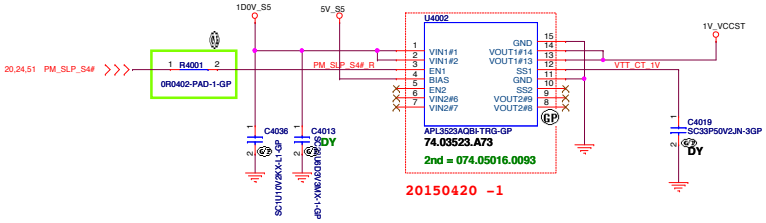
ANNIE Run Power



20150420 -1

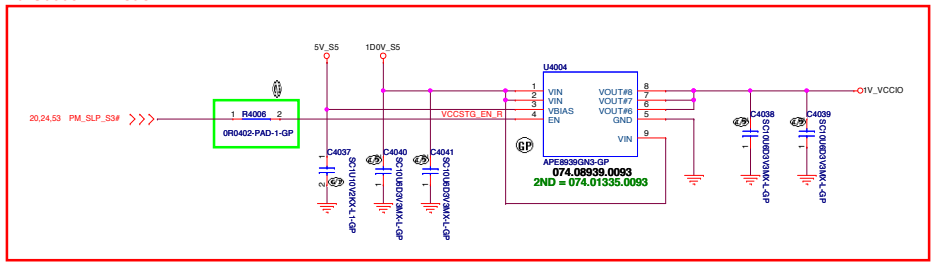
20141022 Jack

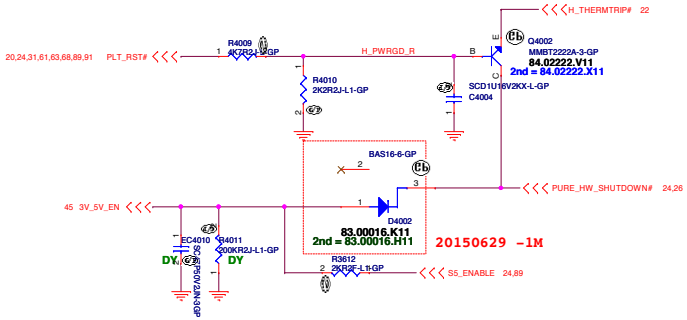
20141022 Jack



20150420 -1

20150608 -1M Jack





20150629 -1M

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<Core Design>

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Title: **Power Plane Enable & SEQUENCE**

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Title **DS3**

Size	Document Number	Rev
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Title **DCIN JACK**

Size	Document Number	Rev
A3	Brook_SLU	1M

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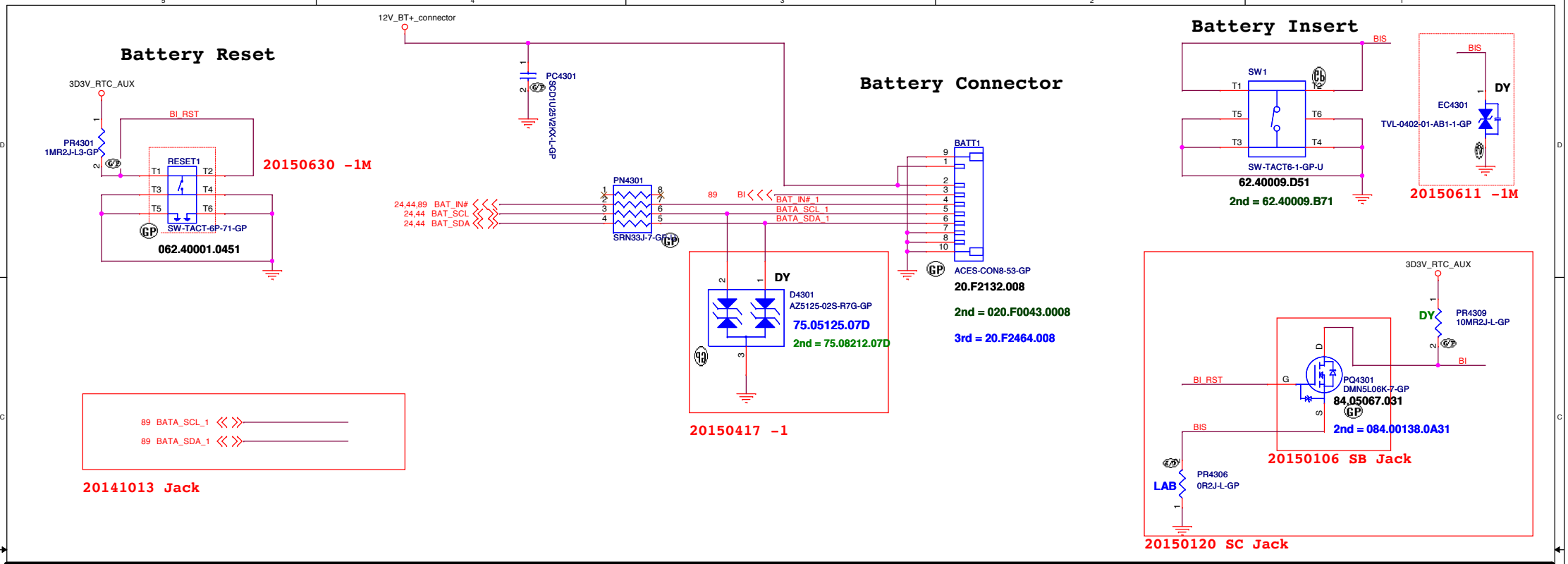

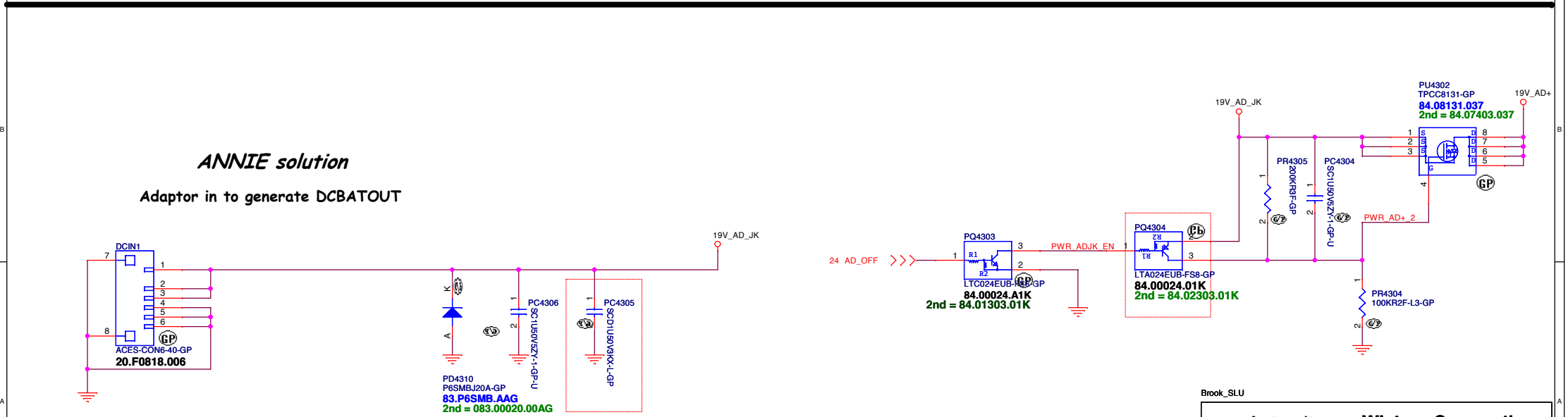

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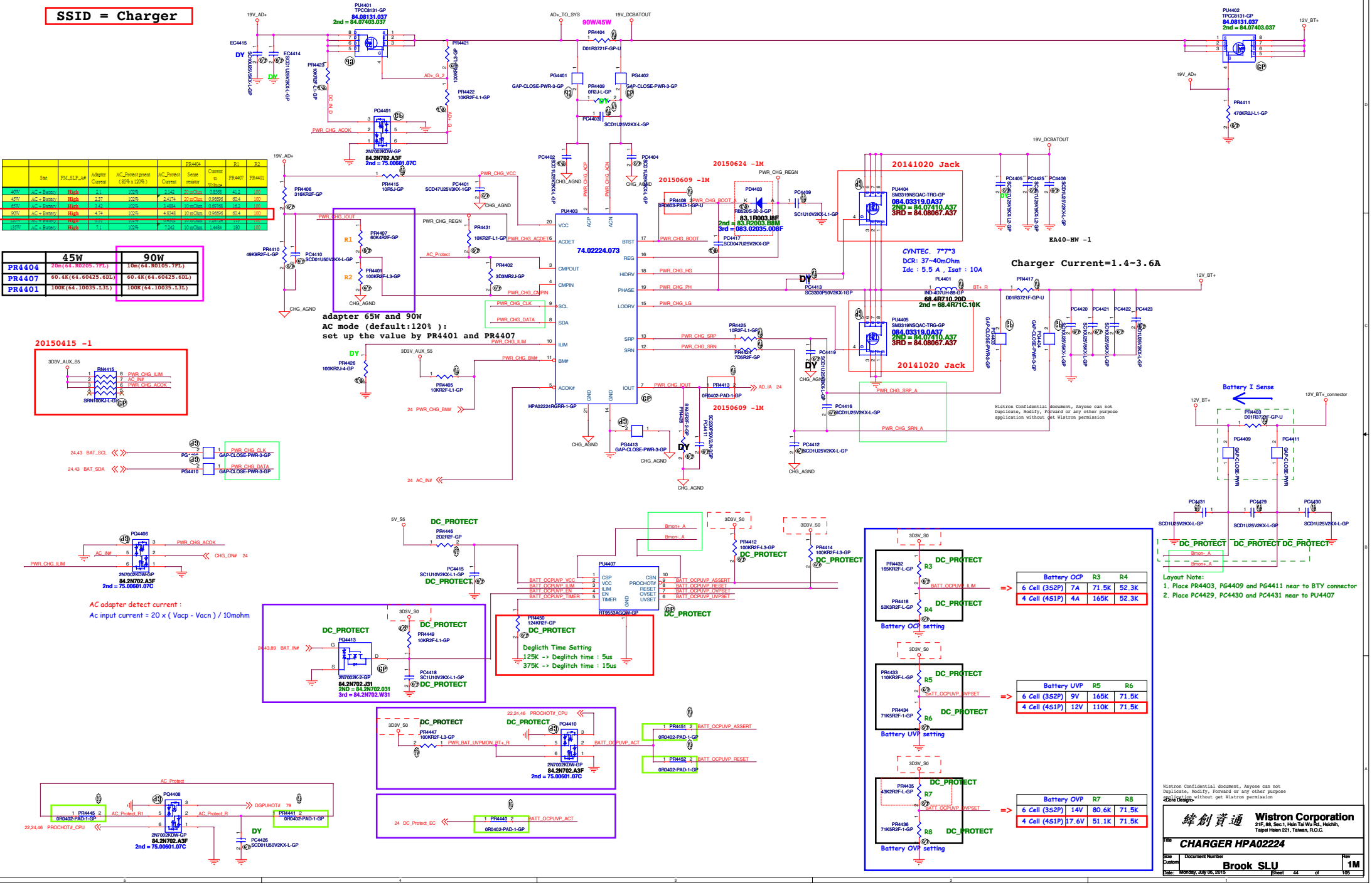
Title	***DC IN/BATT CONN***	
Size A3	Document Number **Brook_SLU**	Rev **1M**
Date: Monday, July 06, 2015	Sheet 43 of 105	

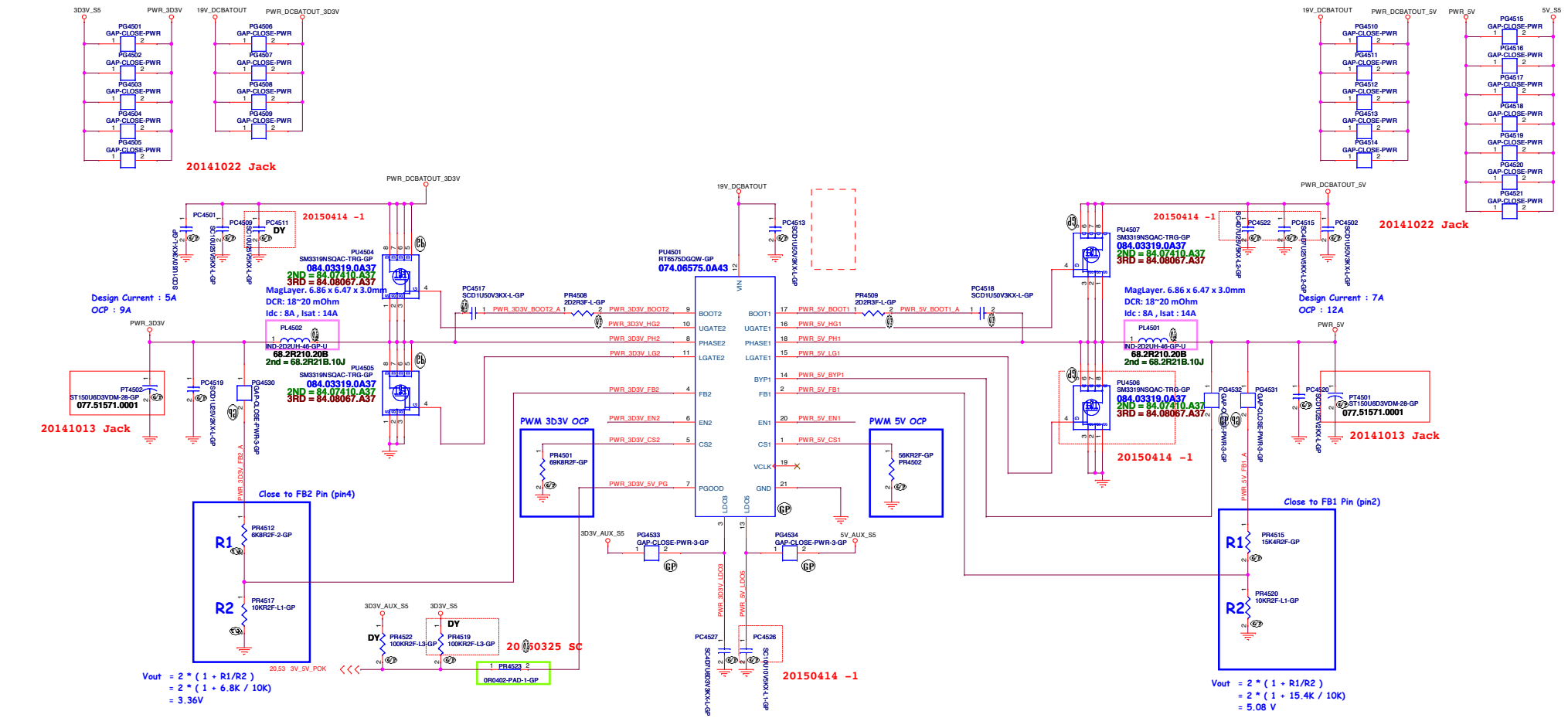
SSID = Charger



	Stat	PM_SLP_A#	Adapter Current	AC_Protect present (85% x 120%)	AC_Protect Current	PR4404 Sense resistor	Current to Voltage	R1 PR4407	R2 PR4401
40W	AC + Battery	High	2.1	100%	2.142	20 mOhm	0.8568	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	20 mOhm	0.96696	60.4	100
65W	AC + Battery	High	3.42	102%	3.4884	10 mOhm	0.69768	60.4	100
90W	AC + Battery	High	4.74	102%	4.8348	10 mOhm	0.96696	60.4	100
90W	AC + Battery	High	4.74	102%	4.8348	10 mOhm	0.96696	60.4	100
135W	AC + Battery	High	7.1	102%	7.242	10 mOhm	1.4484	180	100

	45W	90W
PR4404	20m(64.R0205.7FL)	10m(64.R0105.7FL)
PR4407	60.4K(64.60425.6DL)	60.4K(64.60425.6DL)
PR4401	100K(64.10035.L3L)	100K(64.10035.L3L)

adapter 65W and 90W
AC mode (default:120%):
set up the value by PR4401 and PR4407



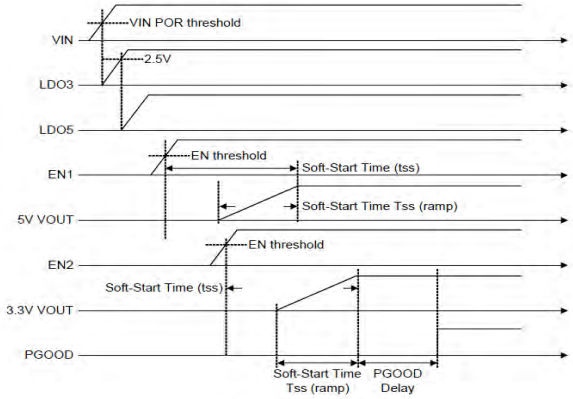


Figure 6. RT6575B Timing

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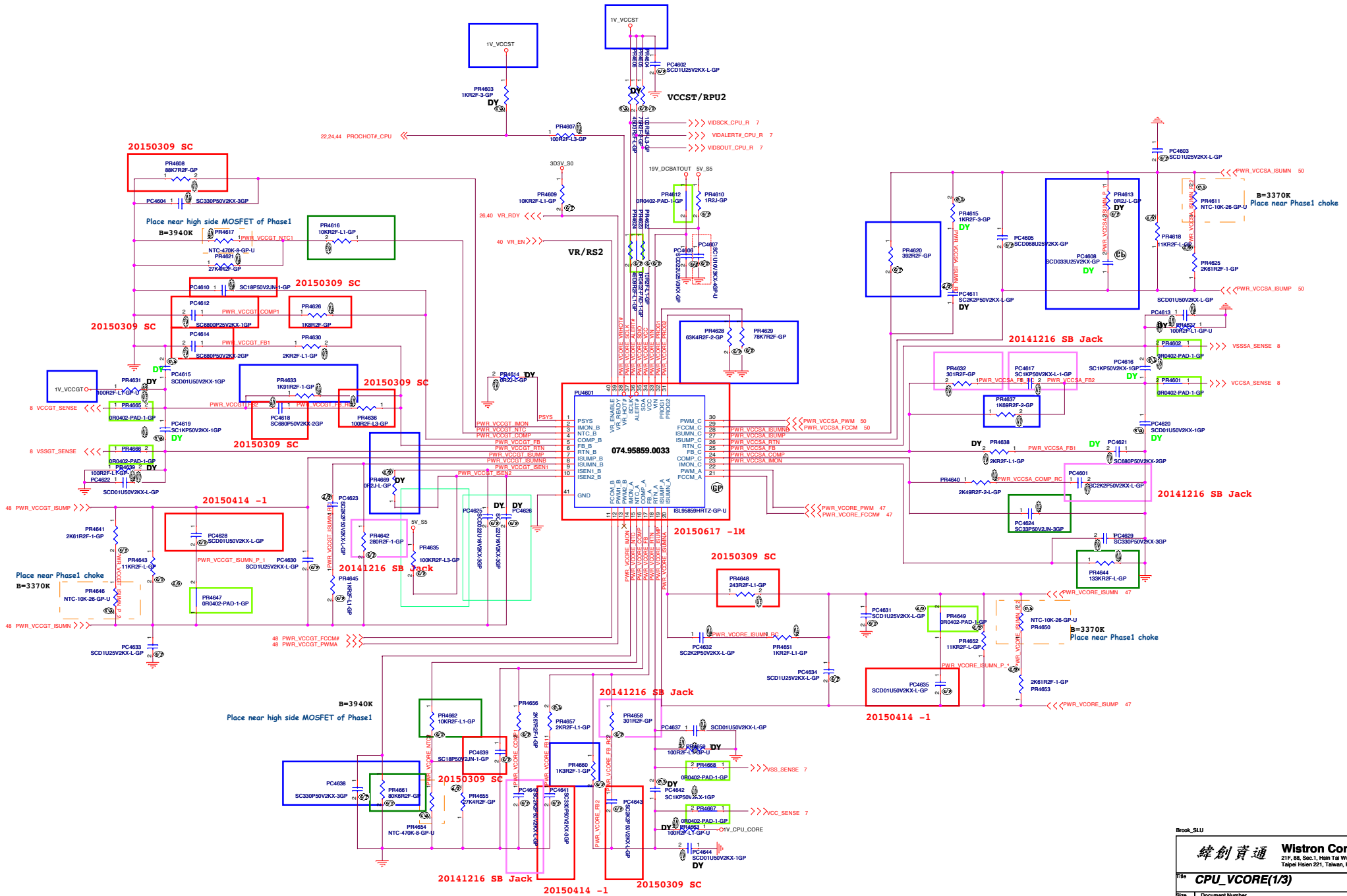
Title: RT6575D_5V/3D3V

Size: A2 | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 06, 2015 | Sheet 45 of 105

Main Func = CPU_CORE



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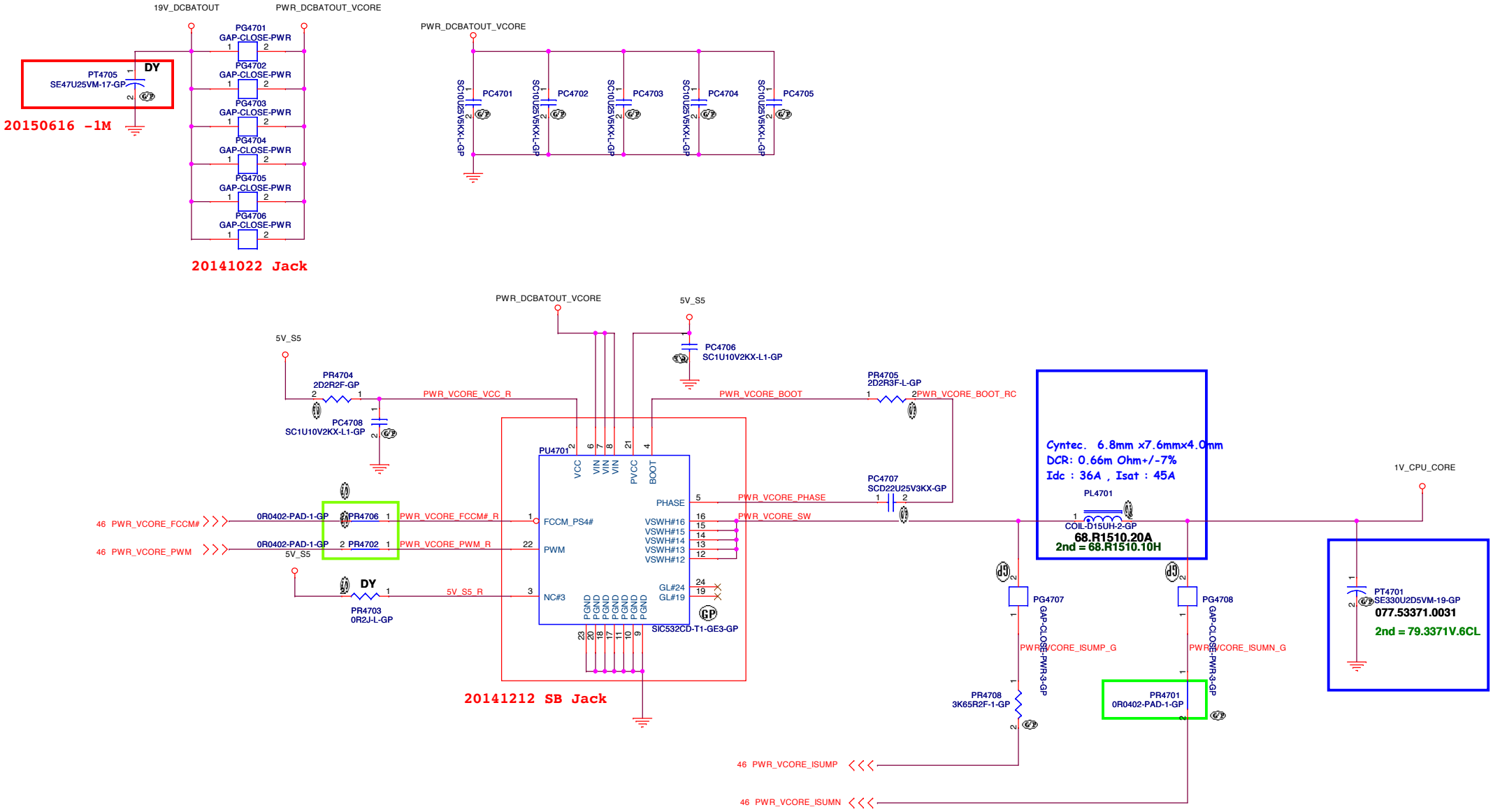
Title: CPU_VCORE(1/3)

Size: A2 | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 06, 2015 | Sheet 46 of 105

Main Func = CPU_CORE



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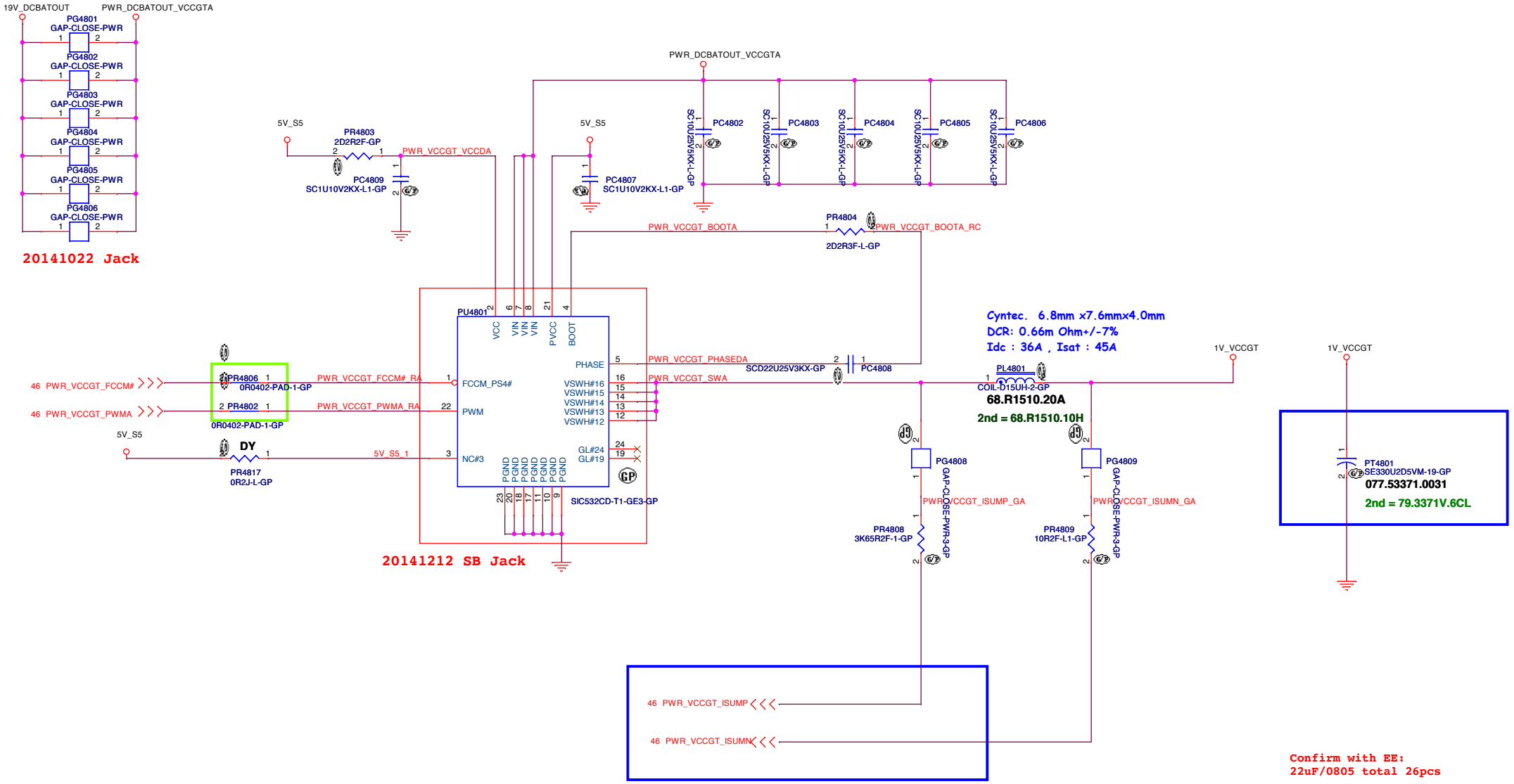
Title	*CPU_VCORE(2/3)*	
Size A3	Document Number **Brook_SLU**	Rev **1M**
Date: Monday, July 06, 2015	Sheet 47 of 105	

Main Func = CPU_CORE



Confirm with EE:
22uF/0805 total 26pcs

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Title	CPU_VCCGT(3/3)	
Size A3	Document Number Brook_SLU	Rev 1M
Date: Monday, July 06, 2015	Sheet 48 of 105	

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Title: ***VCCGTUS***

Size: A2 | Document Number: **Brook_SLU** | Rev: **1M**

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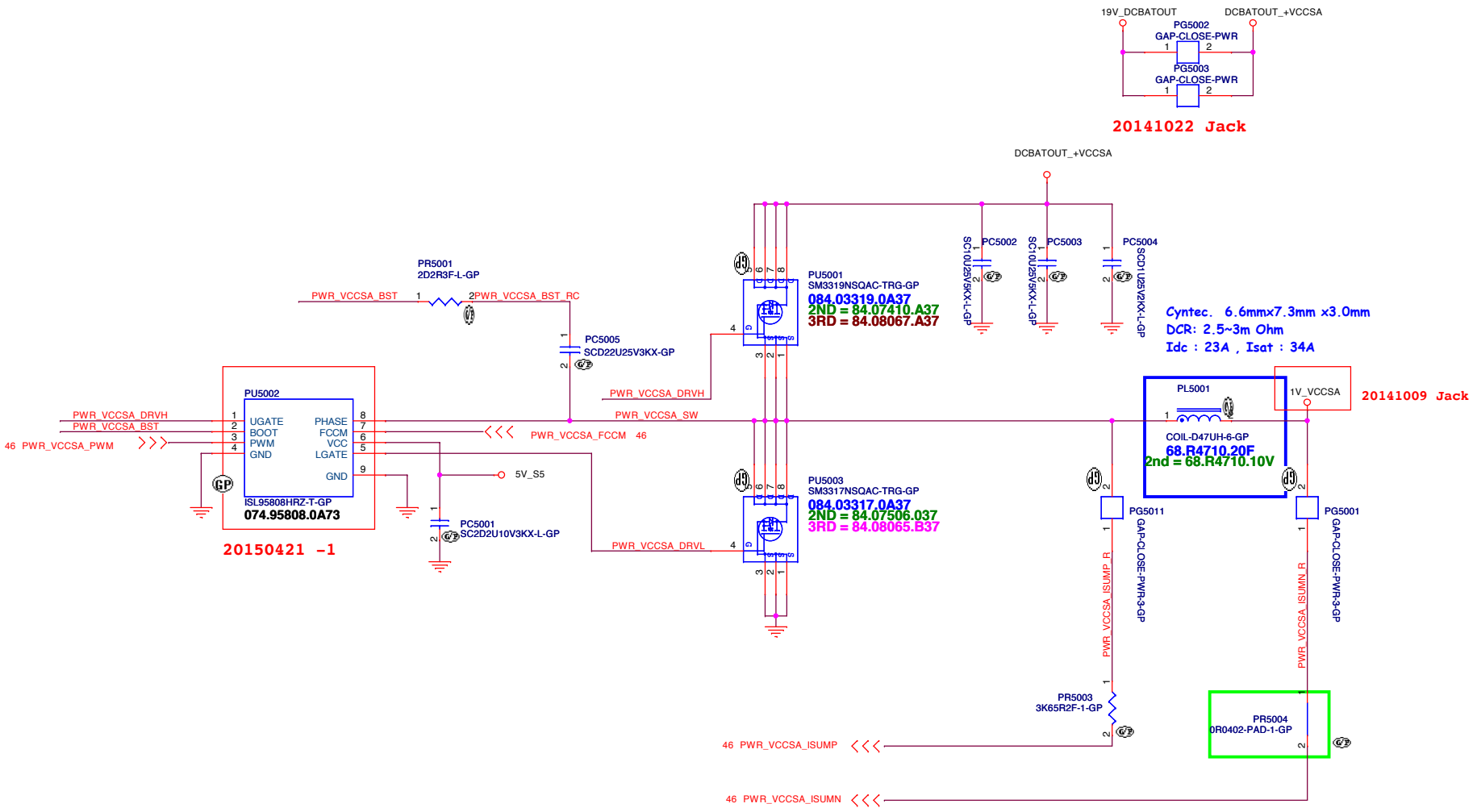
Main Func = CPU_CORE



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Title	***VCCSA***	
Size A3	Document Number **Brook_SLU**	Rev **1M**
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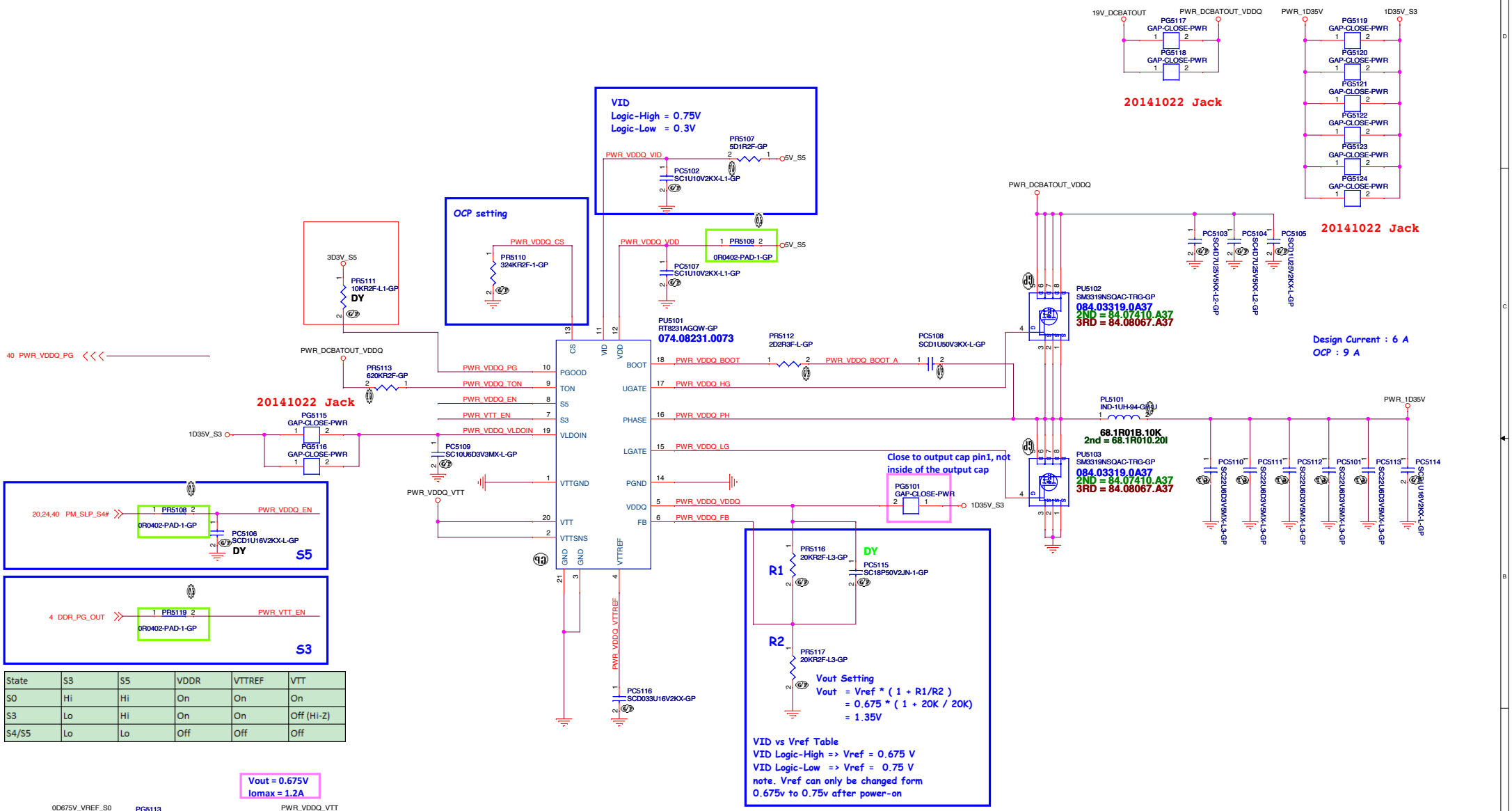
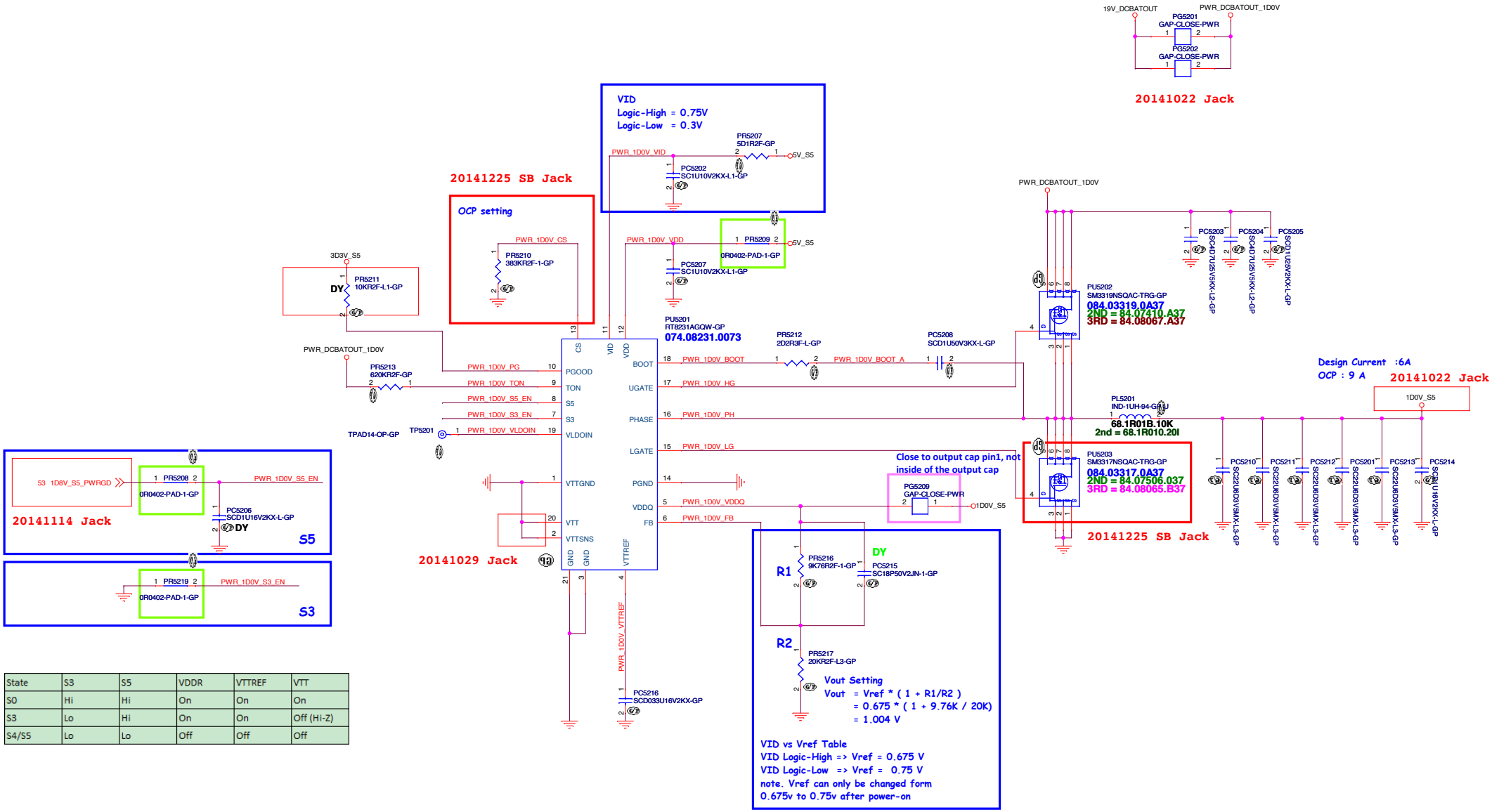


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Brook_SLU

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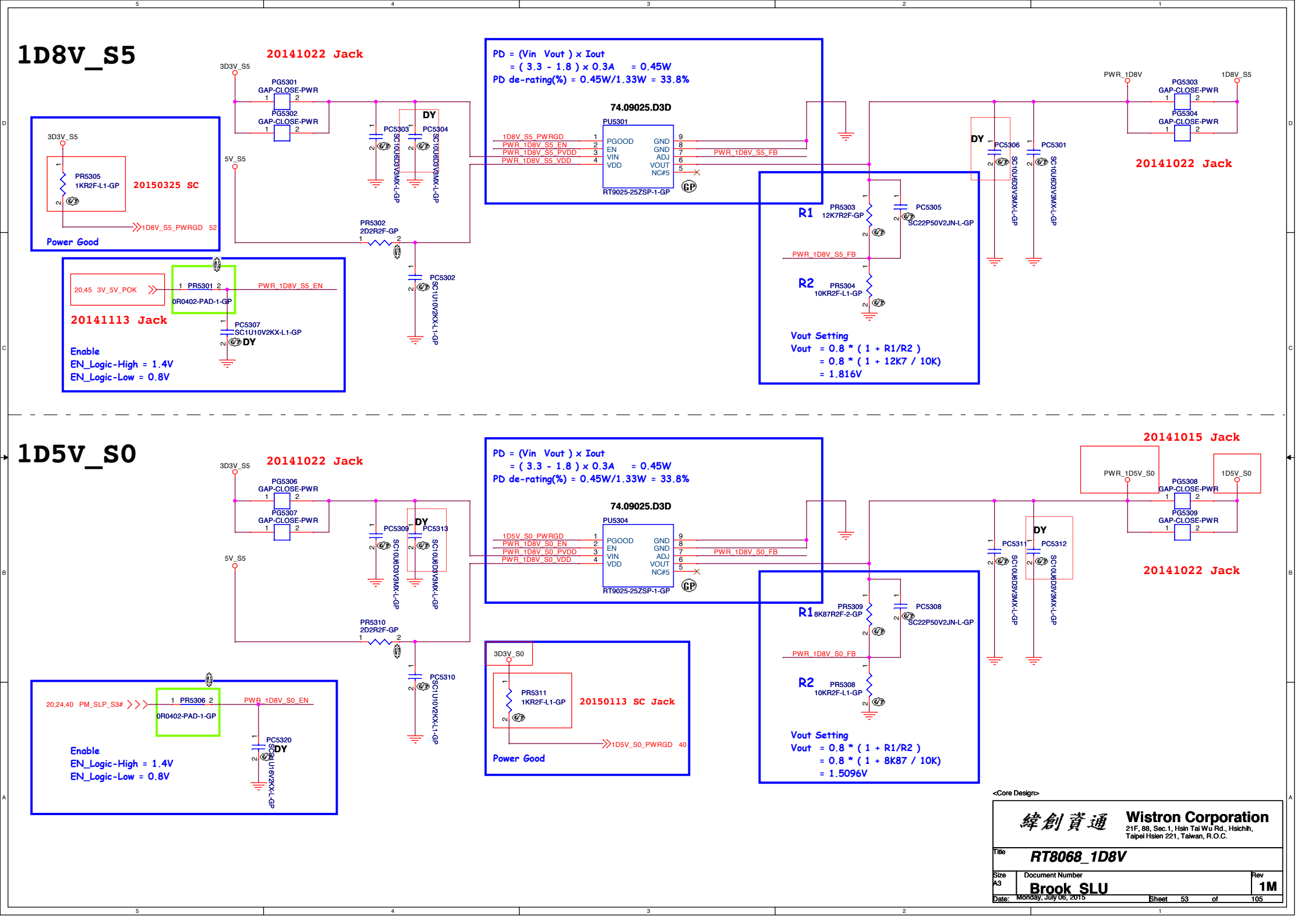
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231_1D0V

Size: Custom | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 06, 2015 | Sheet 52 of 105


1D8V_S5
20141022 Jack
3D3V_S5
PG5301
GAP-CLOSE-PWR
PG5302
GAP-CLOSE-PWR
5V_S5
PC5303
PC5304
DY
SC10U6D3V3MX-L-GP
PR5302
2D2R2F-GP
PC5302
SC1U10V2KX-L1-GP
PD = (Vin Vout) x Iout
= (3.3 - 1.8) x 0.3A = 0.45W
PD de-rating(%) = 0.45W/1.33W = 33.8%
74.09025.D3D
PU5301
1D8V_S5_PWRGD
PWR_1D8V_S5_EN
PWR_1D8V_S5_PVDD
PWR_1D8V_S5_VDD
PGOOD
EN
VIN
VDD
GND
GND
ADJ
VOUT
NC#5
PWR_1D8V_S5_FB
RT9025-25ZSP-1-GP
PWR_1D8V
1D8V_S5
PG5303
GAP-CLOSE-PWR
PG5304
GAP-CLOSE-PWR
20141022 Jack
PC5306
PC5301
R1
PR5303
12K7R2F-GP
PC5305
SC22P50V2JN-L-GP
PWR_1D8V_S5_FB
R2
PR5304
10KR2F-L1-GP
Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V
3D3V_S5
PR5305
1KR2F-L1-GP
20150325 SC
1D8V_S5_PWRGD 52
Power Good
20,45 3V_5V_POK
PR5301
0R0402-PAD-1-GP
PWR_1D8V_S5_EN
20141113 Jack
PC5307
SC1U10V2KX-L1-GP
DY
Enable
EN_Logic-High = 1.4V
EN_Logic-Low = 0.8V
1D5V_S0
20141022 Jack
3D3V_S5
PG5306
GAP-CLOSE-PWR
PG5307
GAP-CLOSE-PWR
5V_S5
PC5309
PC5313
DY
SC10U6D3V3MX-L-GP
PR5310
2D2R2F-GP
PC5310
SC1U10V2KX-L1-GP
PD = (Vin Vout) x Iout
= (3.3 - 1.8) x 0.3A = 0.45W
PD de-rating(%) = 0.45W/1.33W = 33.8%
74.09025.D3D
PU5304
1D5V_S0_PWRGD
PWR_1D8V_S0_EN
PWR_1D8V_S0_PVDD
PWR_1D8V_S0_VDD
PGOOD
EN
VIN
VDD
GND
GND
ADJ
VOUT
NC#5
PWR_1D8V_S0_FB
RT9025-25ZSP-1-GP
20141015 Jack
PWR_1D5V_S0
1D5V_S0
PG5308
GAP-CLOSE-PWR
PG5309
GAP-CLOSE-PWR
20141022 Jack
PC5311
PC5312
DY
SC10U6D3V3MX-L-GP
R1
PR5309
8K87R2F-2-GP
PC5308
SC22P50V2JN-L-GP
PWR_1D8V_S0_FB
R2
PR5308
10KR2F-L1-GP
Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 8K87 / 10K)
= 1.5096V
3D3V_S0
PR5311
1KR2F-L1-GP
20150113 SC Jack
1D5V_S0_PWRGD 40
Power Good
20,24,40 PM_SLP_S3#
PR5306
0R0402-PAD-1-GP
PWR_1D8V_S0_EN
PC5320
SC1U16V2KX-L-GP
DY
Enable
EN_Logic-High = 1.4V
EN_Logic-Low = 0.8V
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8068_1D8V
Size
A3
Document Number
Brook_SLU
Rev
1M
Date: Monday, July 06, 2015
Sheet 53 of 105

Brook_SLU

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Title ***Reserved***

Size	Document Number	Rev
A4	**Brook_SLU**	**1M**

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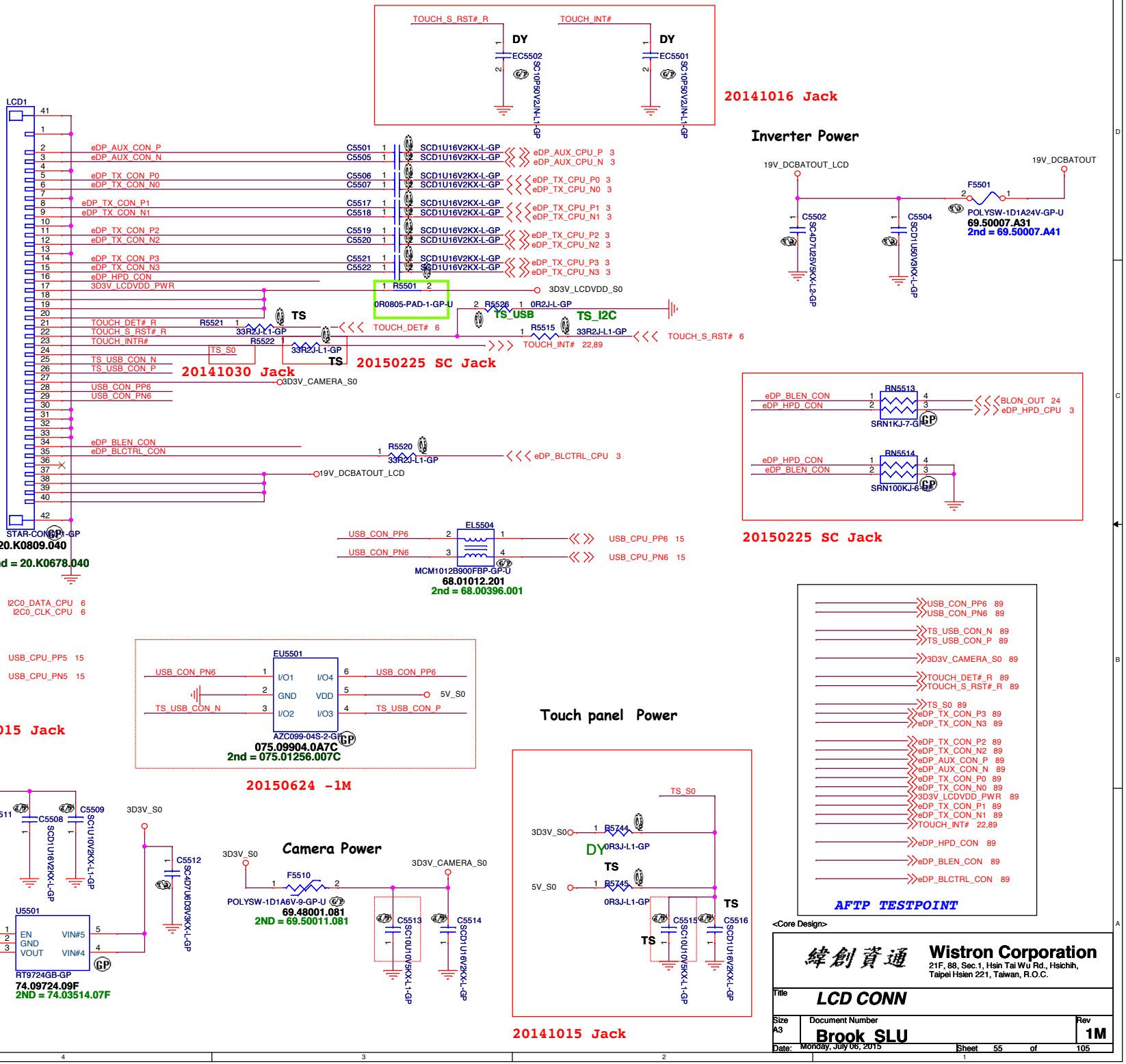
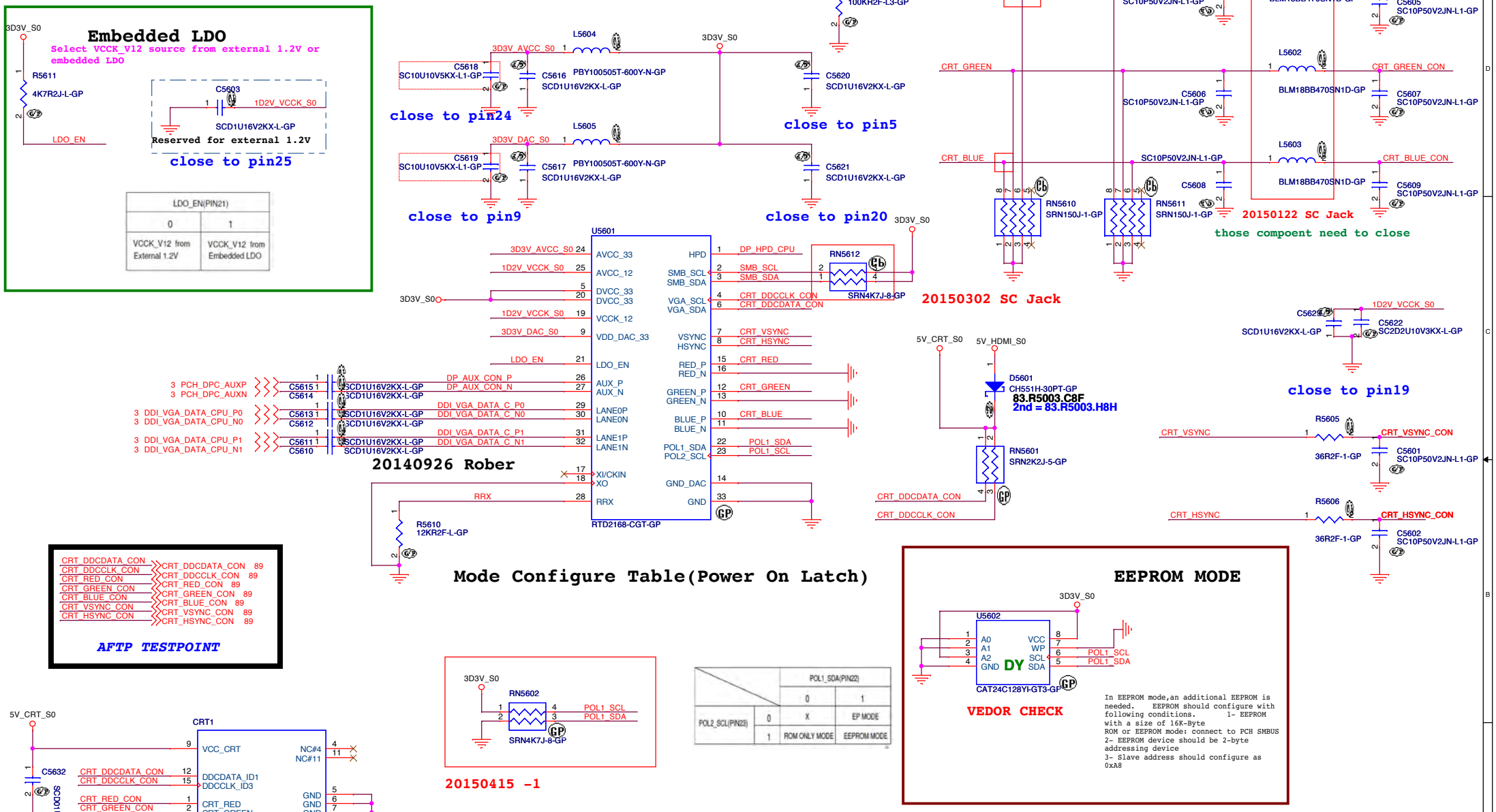
Main Func = LCD

Pin count		
1	Display	EDP 4Lane+CCD
2		GND
3		eDP_AUX_CON_P
4		eDP_AUX_CON_N
5		GND
6		eDP_TX_CON_P0
7		eDP_TX_CON_N0
8		GND
9		eDP_TX_CON_P1
10		eDP_TX_CON_N1
11		GND
12		eDP_TX_CON_P2
13		eDP_TX_CON_N2
14		GND
15		eDP_TX_CON_P3
16		eDP_TX_CON_N3
17		eDP_HPD_CON
18		LCDVDD(3V)
19		LCDVDD(3V)
20		LCDVDD(3V)
21		LCDVDD(3V)
22	Touch	TOUCH_DET#
23		TOUCH_GND/ TOUCH_RST
24		TOUCH_EN/ TOUCH_INT
25		Touch_PWR(3V/5V)
26		USB_PN6/ SCL
27		USB_PP6/ SDA
28	CCD	3D3V_CAMERA_S0
29		USB_CAMERA_P
30		USB_CAMERA_N
31	GND	GND
32		GND
33		GND
34		GND
35		
36		
37		
38	DCBATOUT	DCBATOUT_LCD
39		DCBATOUT_LCD
40		DCBATOUT_LCD
		DCBATOUT_LCD



SSID = Display

VGA RTD2168



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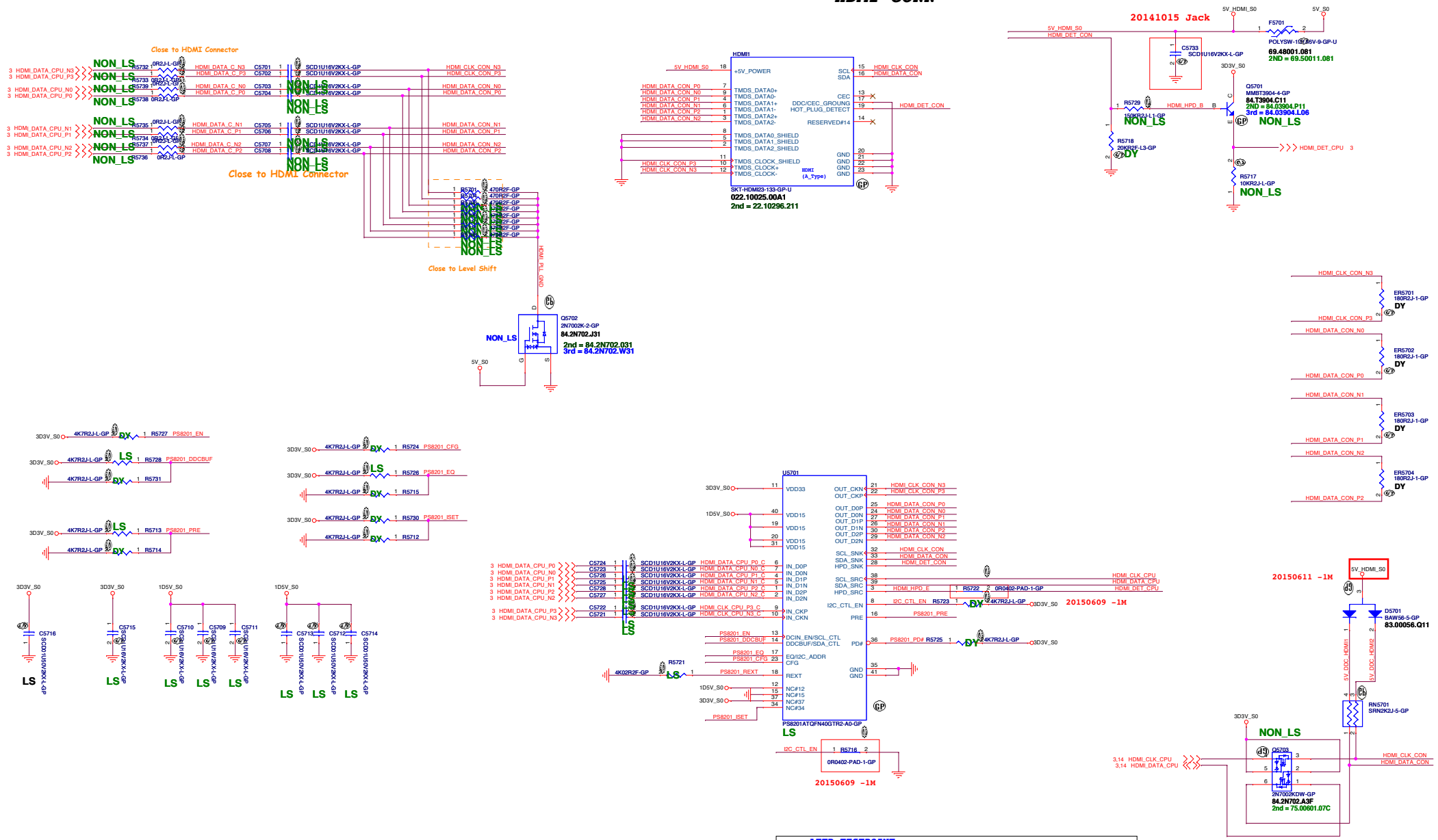
Title	*VGA RTD2168*	
Size A3	Document Number **Brook_SLU**	Rev **1M**
Date: Monday, July 06, 2015	Sheet 56 of 105	

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN



AFTP TESTPOINT

HDMI_DATA_CON_P0	HDMI_DATA_CON_P0 89	HDMI_CLK_CON	HDMI_CLK_CON 89
HDMI_DATA_CON_N0	HDMI_DATA_CON_N0 89	HDMI_DATA_CON	HDMI_DATA_CON 89
HDMI_DATA_CON_P1	HDMI_DATA_CON_P1 89	HDMI_DET_CON	HDMI_DET_CON 89
HDMI_DATA_CON_N1	HDMI_DATA_CON_N1 89		
HDMI_DATA_CON_P2	HDMI_DATA_CON_P2 89		
HDMI_DATA_CON_N2	HDMI_DATA_CON_N2 89		
HDMI_CLK_CON_P3	HDMI_CLK_CON_P3 89		
HDMI_CLK_CON_N3	HDMI_CLK_CON_N3 89		

<Core Design>

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Title: HDMI Level Shifter/Connector

Size: A2 | Document Number: Brook_SLU | Rev: 1M

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緯創資通 **Wistron Corporation**
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Title		
Size A	Document Number **Brook_SLU**	Rev **1M**
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Title	DVI	
Size A	Document Number Brook_SLU	Rev 1M
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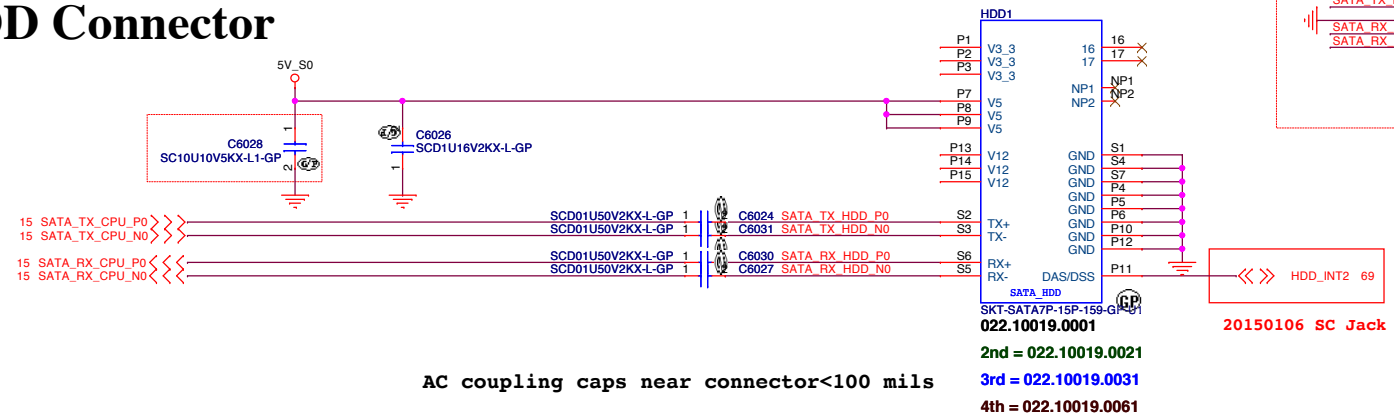
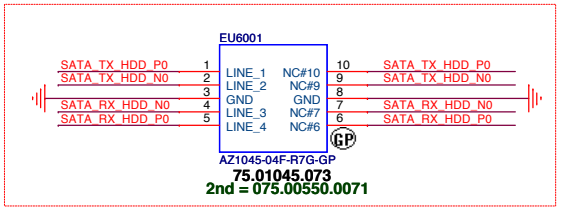
SSID = SATA

SATA HDD Connector

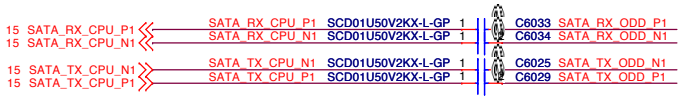


AC coupling caps near connector<100 mils

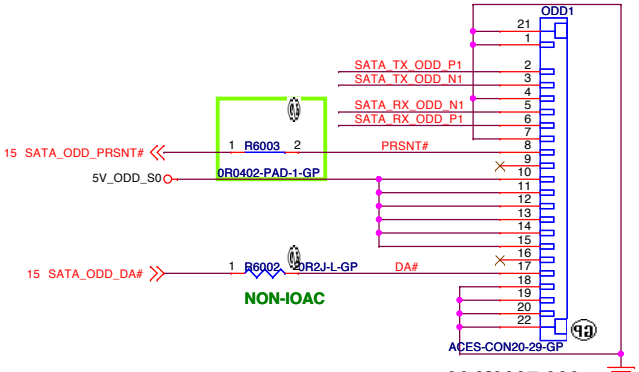


20150624 -1M

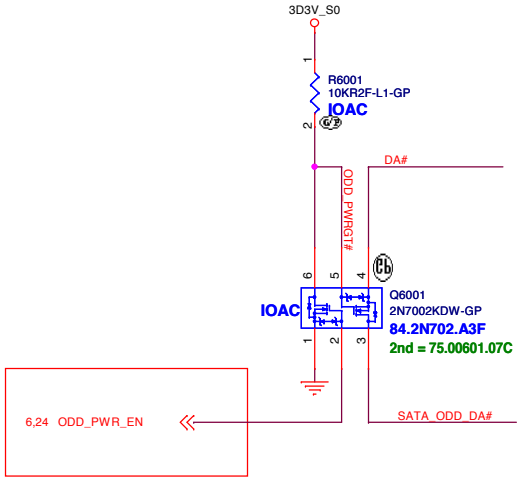
SATA ODD Connector

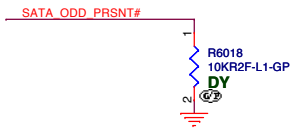


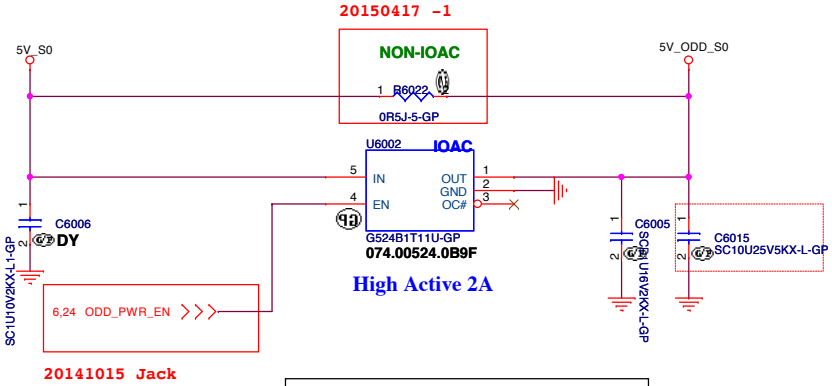
AC coupling caps near connector<100 mils



PIN DEFINE	CONN	FFC
GND	P5/P6	20
GND		19
GND		18
ODD_DA	P4	17
NC		16
5V	P2/P3	15
5V		14
5V		13
5V		12
5V		11
5V		10
NC		9
PRSNT	P1	8
GND	S7	7
RXP	S6	6
RXN	S5	5
GND	S4	4
TXN	S3	3
TXP	S2	2
GND	S1	1







AFTP TESTPOINT

SATA_TX_ODD_P1	SATA_TX_ODD_P1 89
SATA_TX_ODD_N1	SATA_TX_ODD_N1 89
SATA_RX_ODD_N1	SATA_RX_ODD_N1 89
SATA_RX_ODD_P1	SATA_RX_ODD_P1 89
PRSNT#	PRSNT# 89
DA#	DA# 89

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Title: HDD / ODD

Size: A3 | Document Number: Brook_SLU | Rev: 1M

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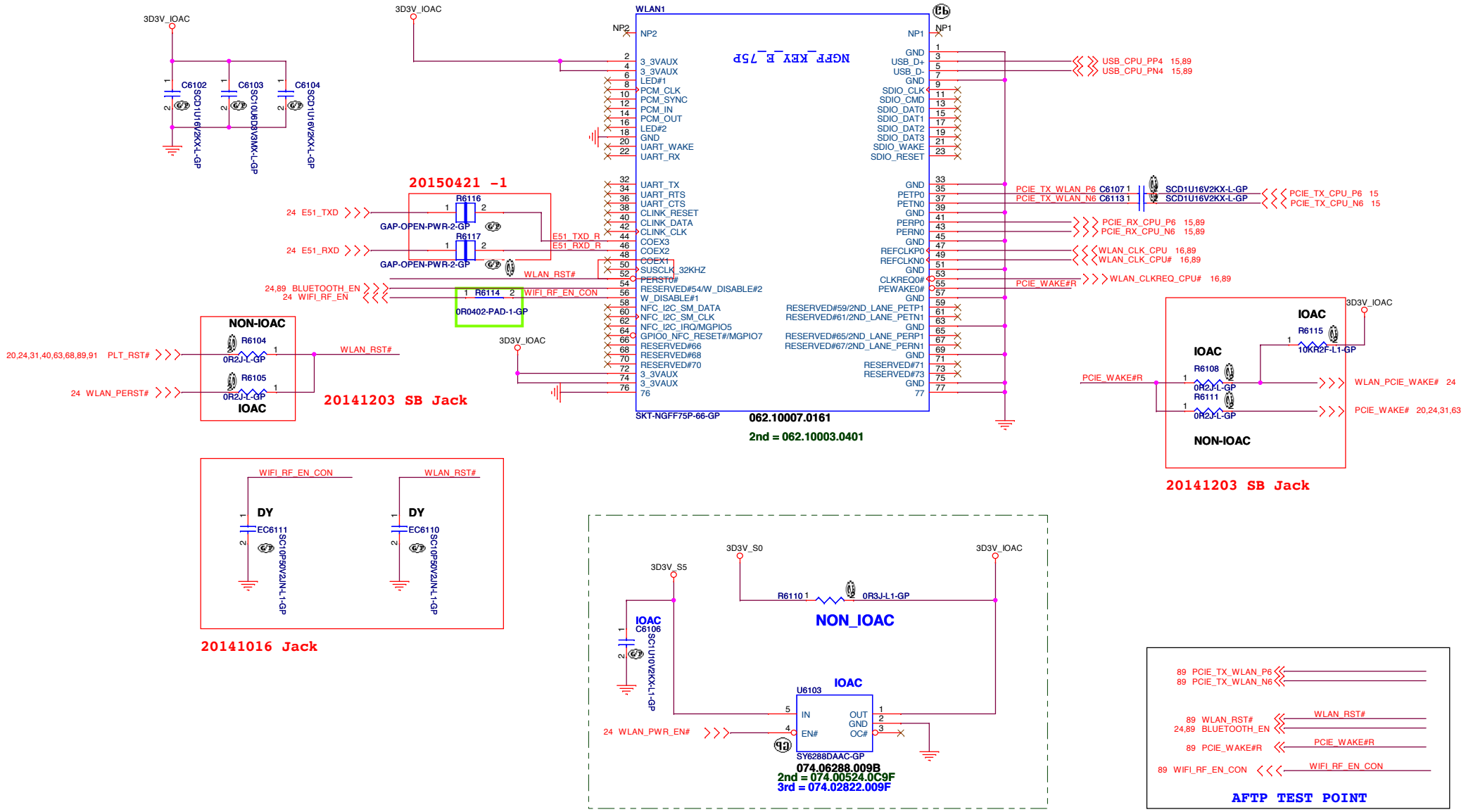
SSID = Wireless Mini Card Connector(802.11a/b/g/n)



Brook_SLU

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Mini Card-WLAN***
Size A3	Document Number **Brook_SLU** Rev **1M**
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Brook_SLU

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Wireless Charging***	
Size A	Document Number **Brook_SLU**	Rev **1M**
Date: Monday, July 06, 2015	Sheet 62 of 105	

SSID = mSATA

Mini Card Connector(mSATA)

17.2.6 General Guidelines for mSATA (Gen 2 and Gen 3) Routing on SATA/PCIe muxed Ports

The below table summarizes the AC cap requirements on the motherboard when using the SATA/PCIe muxed ports.

Table 17-6. SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF[2]	None[3]

Notes:
1. For PCIe only application, please refer to the PCIe guidelines for details.
2. For SATA only application, both PCH Tx and PCH Rx channels need to have 10 nF caps on the motherboard. This option supports all SATA devices. However, the PCH Rx 10 nF capacitor can be removed if DC coupled ODDs/devices are NOT used.
3. For PCIe/SATA muxed application, a 100 nF AC cap is required on motherboards for PCH Tx channel and NO AC cap is required on motherboard for the PCH Rx channel. This option DOES NOT support DC coupled ODDs/Devices.

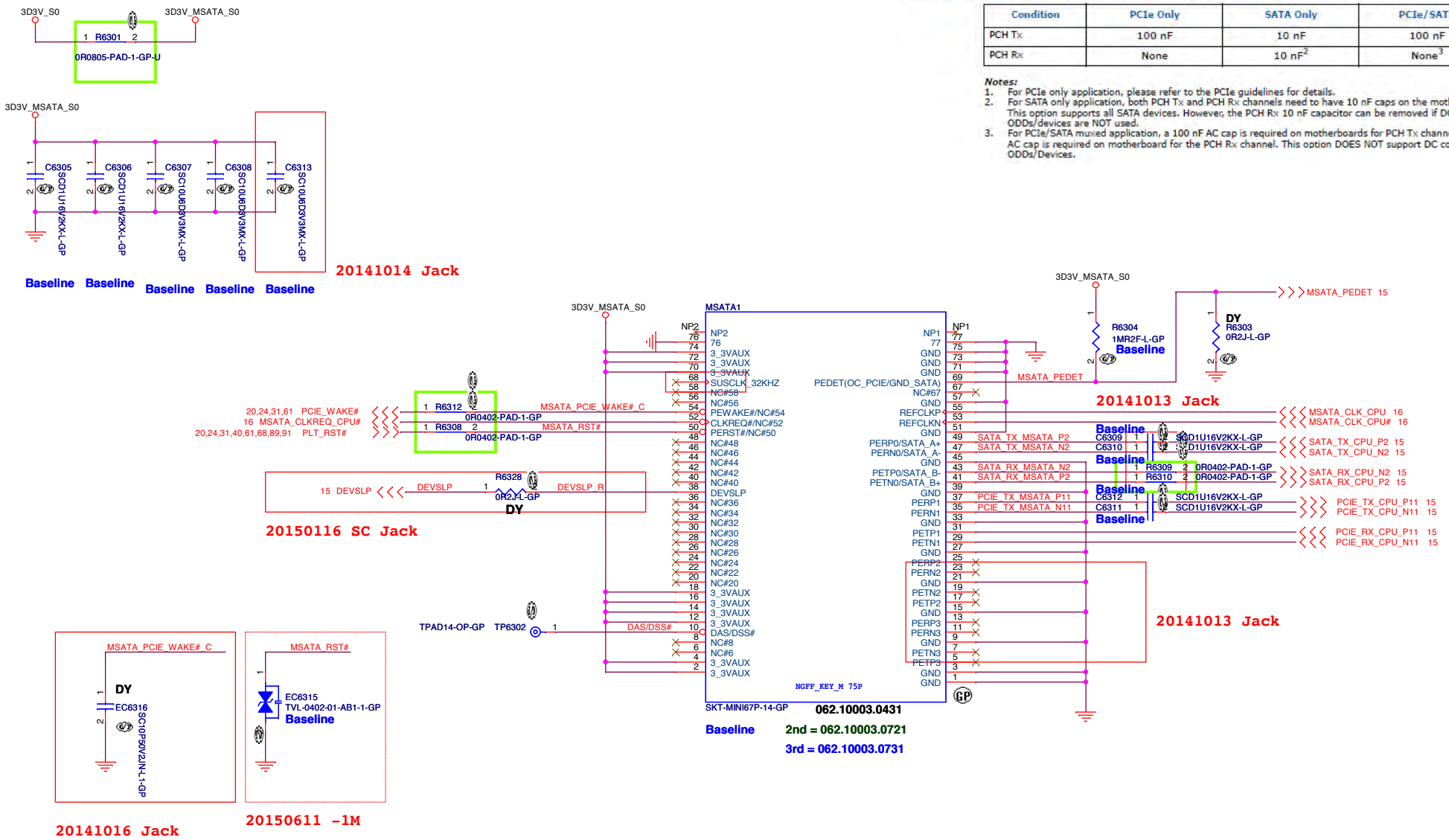

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Brook_SLU

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Title: mSTAT
Size: A3
Document Number: Brook_SLU
Rev: 1M
Date: Monday, July 06, 2015
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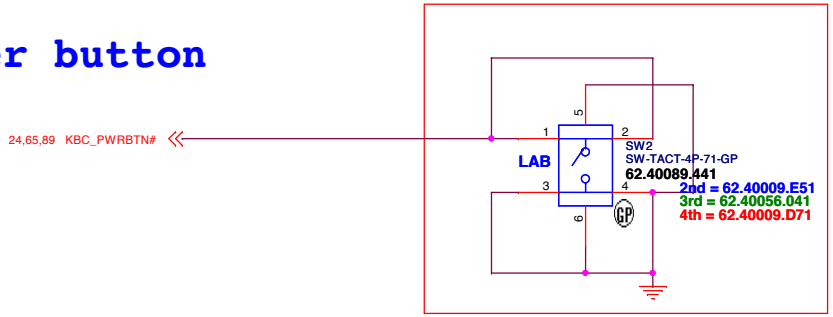
Main Func = Power BTN

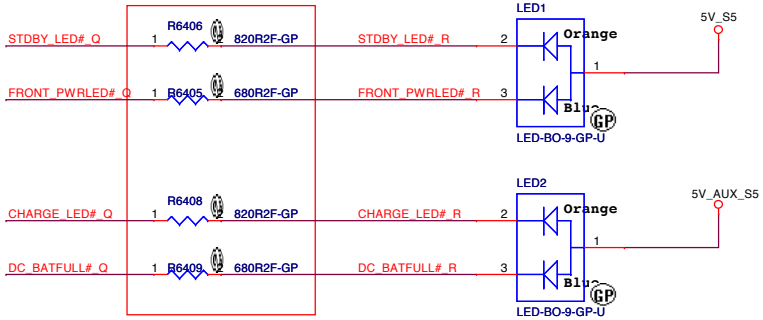
Power button

20140924

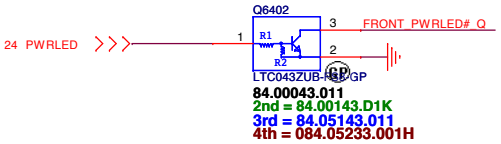


Main Func = Battery LED

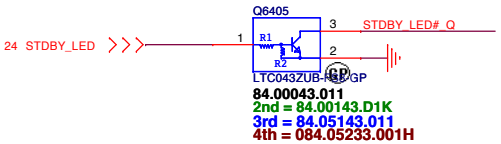
20150113 SC Jack



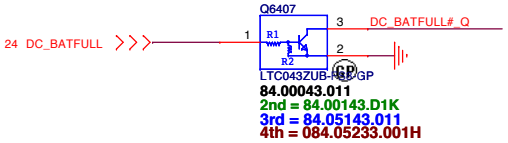
Power Button_LED



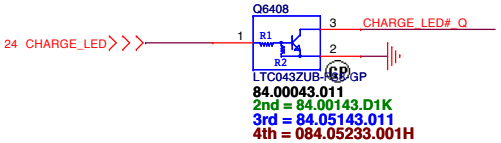
Power STDBY_LED



Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



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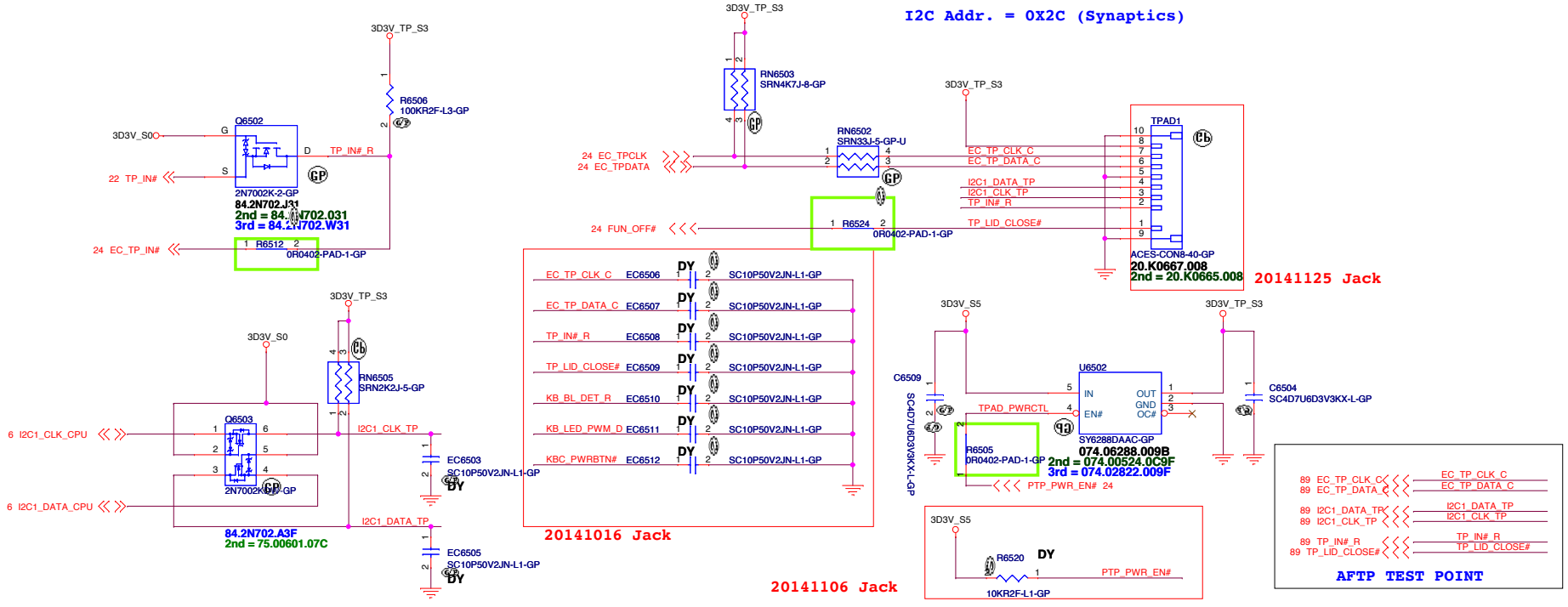
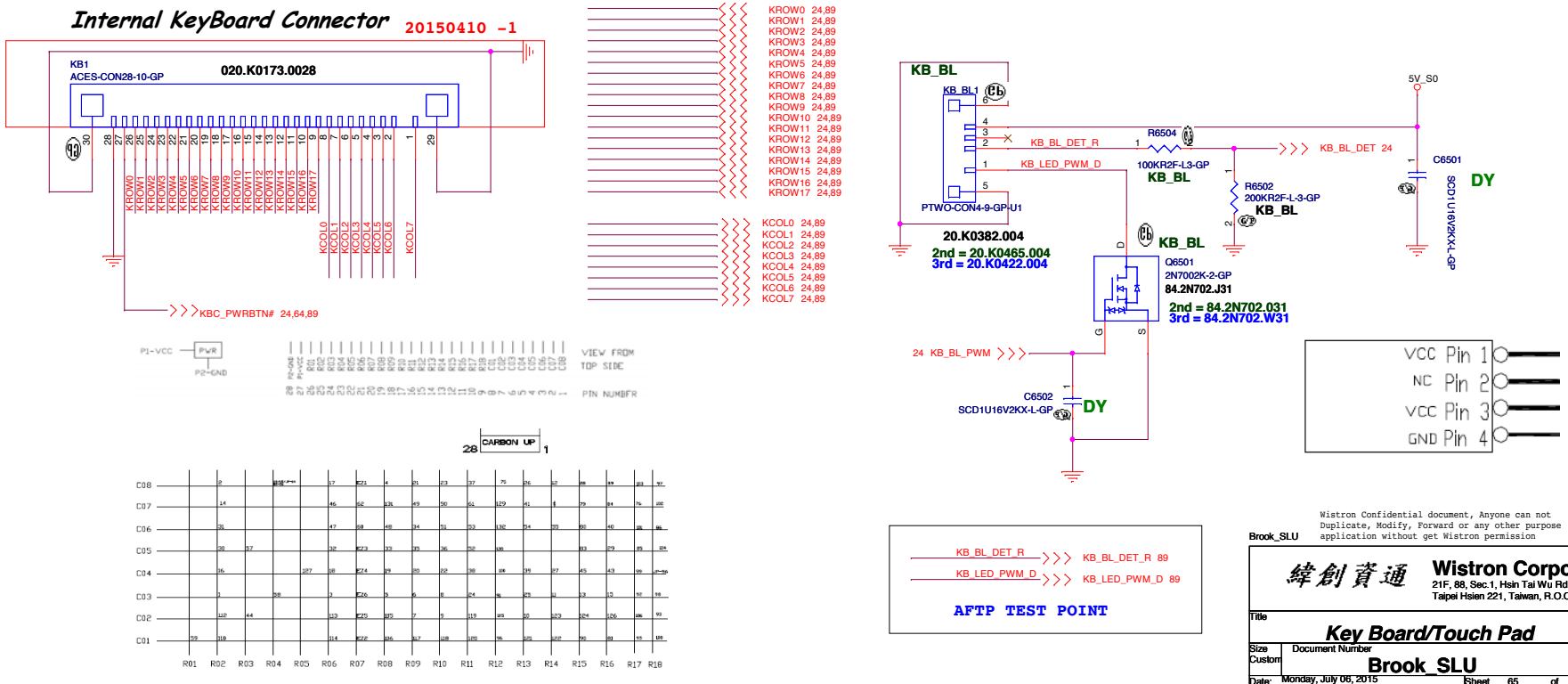
Precision Touch Pad

I2C Addr. = 0X2C (Synaptics)



Internal KeyBoard Connector

20150410 -1



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Size	Document Number	Rev
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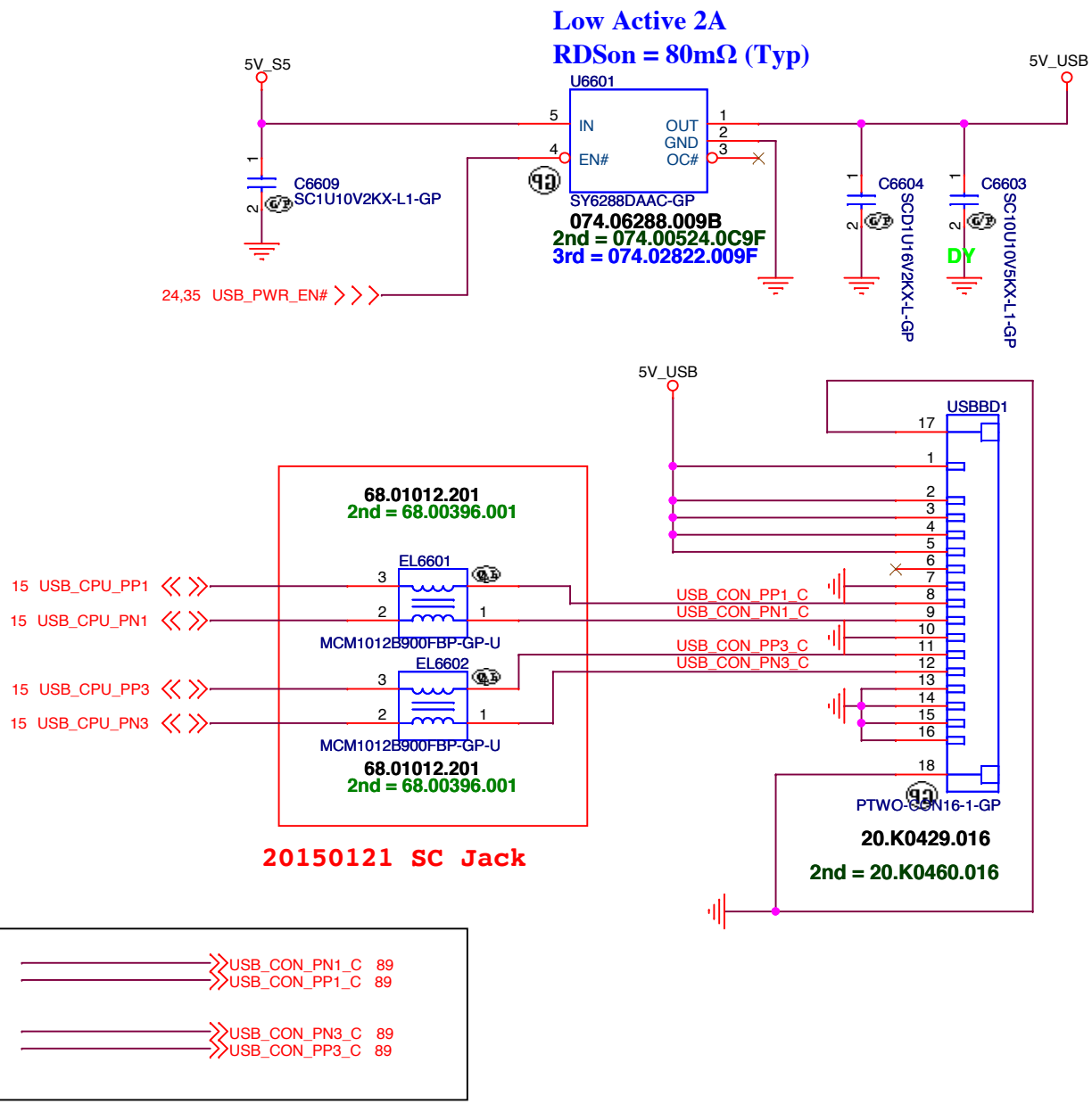

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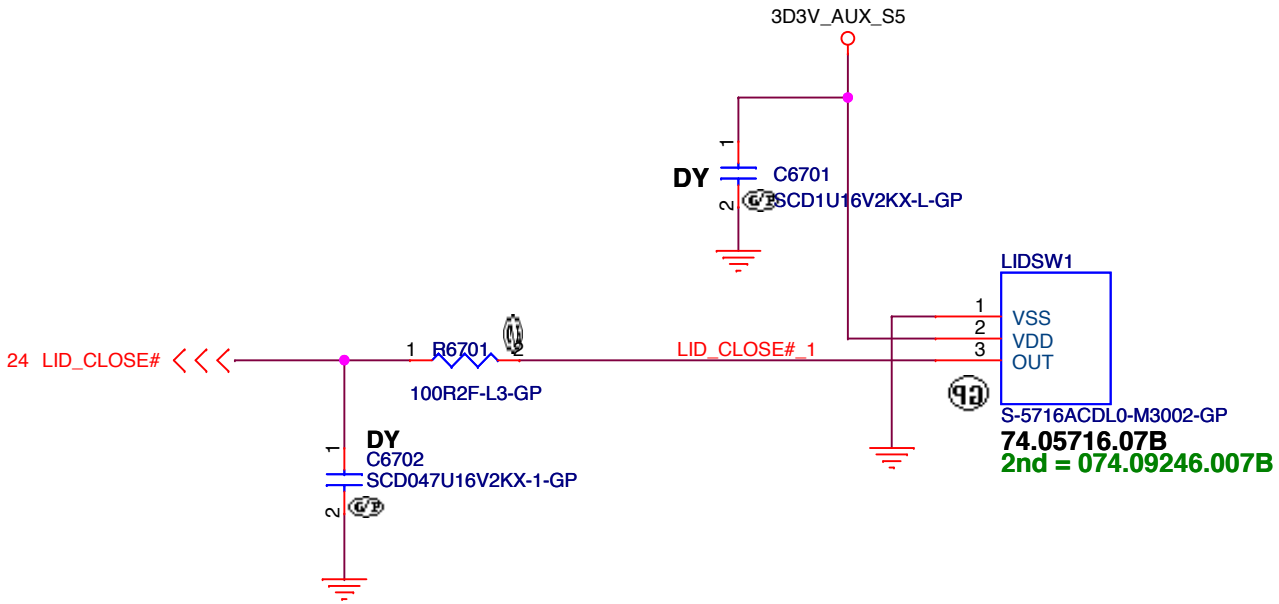

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Title: **Security Guard connector**

Size	Document Number	Rev
A	Brook_SLU	1M

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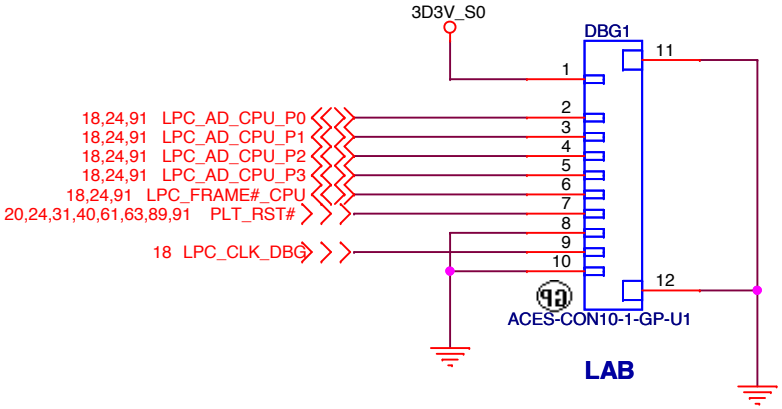

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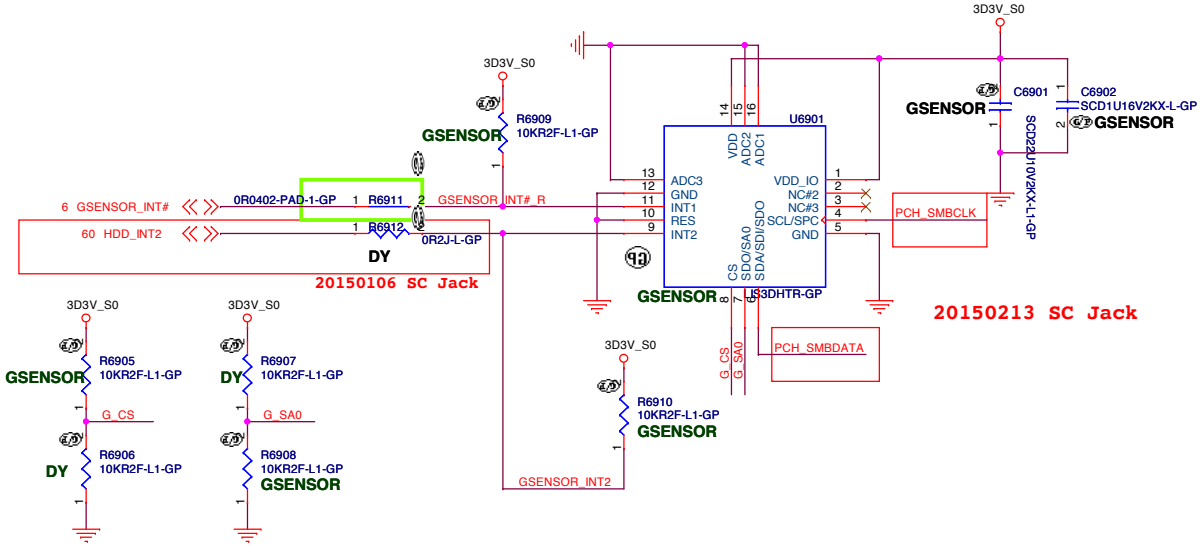
SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

20150213 SC Jack




```
SDO="H"; address="3Ah"
*SDO="L"; address="38h"
```

```
*CS="H"; mode="I2C"
CS="L"; mode="SPI"
```

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Title: ***Hall Sensor***

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Title	***Thunderbolt (5/5)***	
Size A4	Document Number **Brook_SLU**	Rev **1M**
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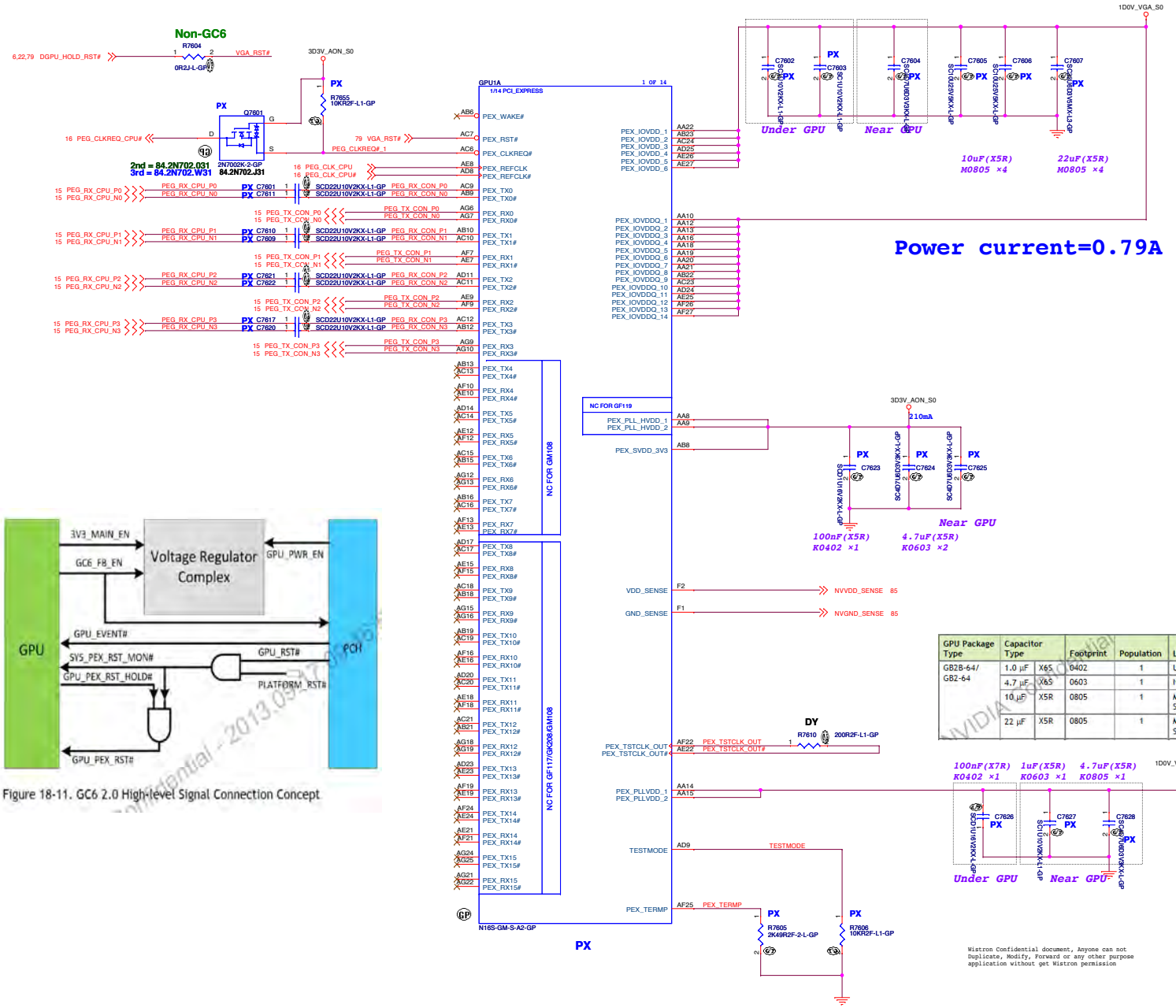

Figure 18-11. GC6 2.0 High-level Signal Connection Concept

3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3B-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

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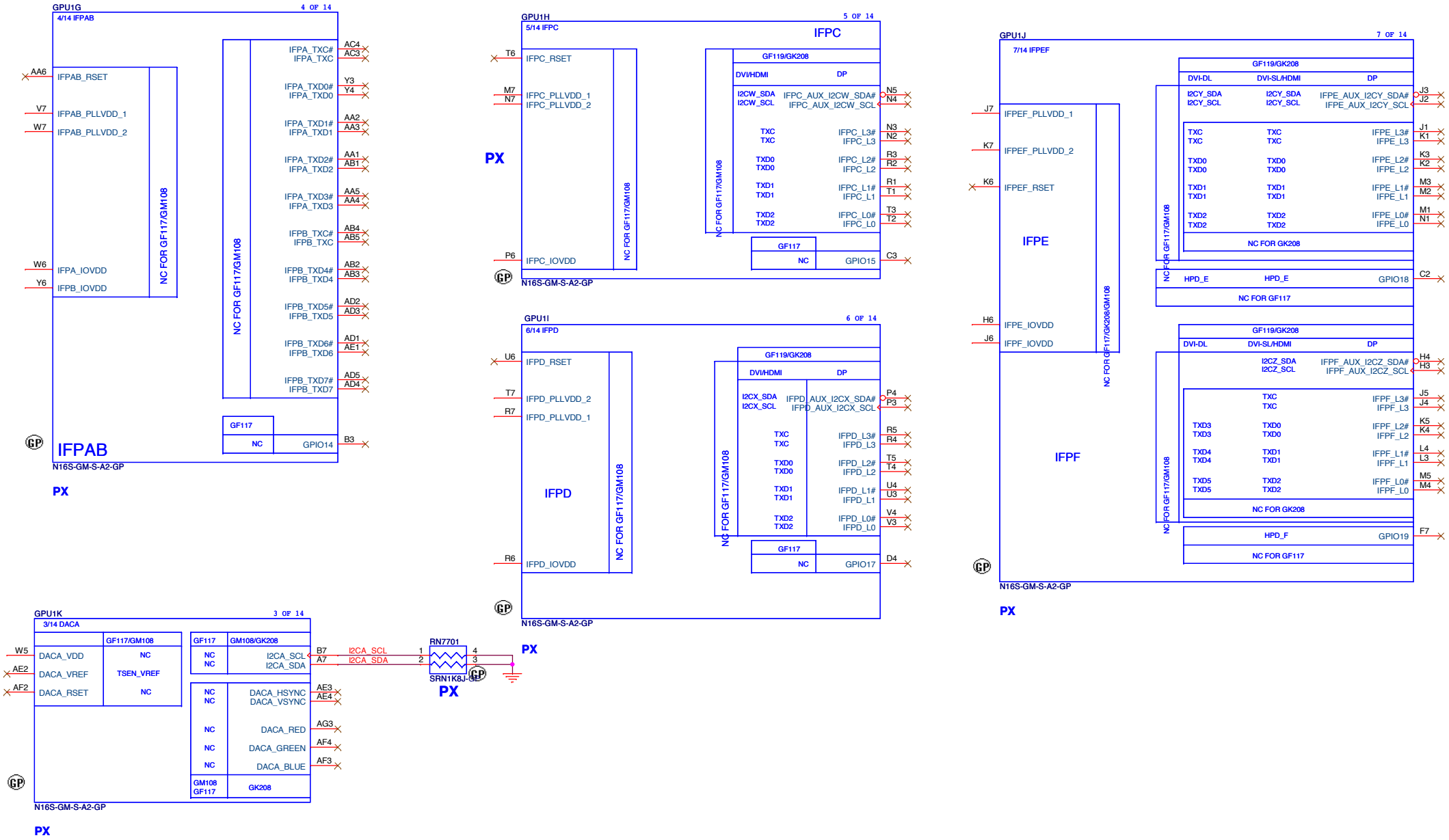

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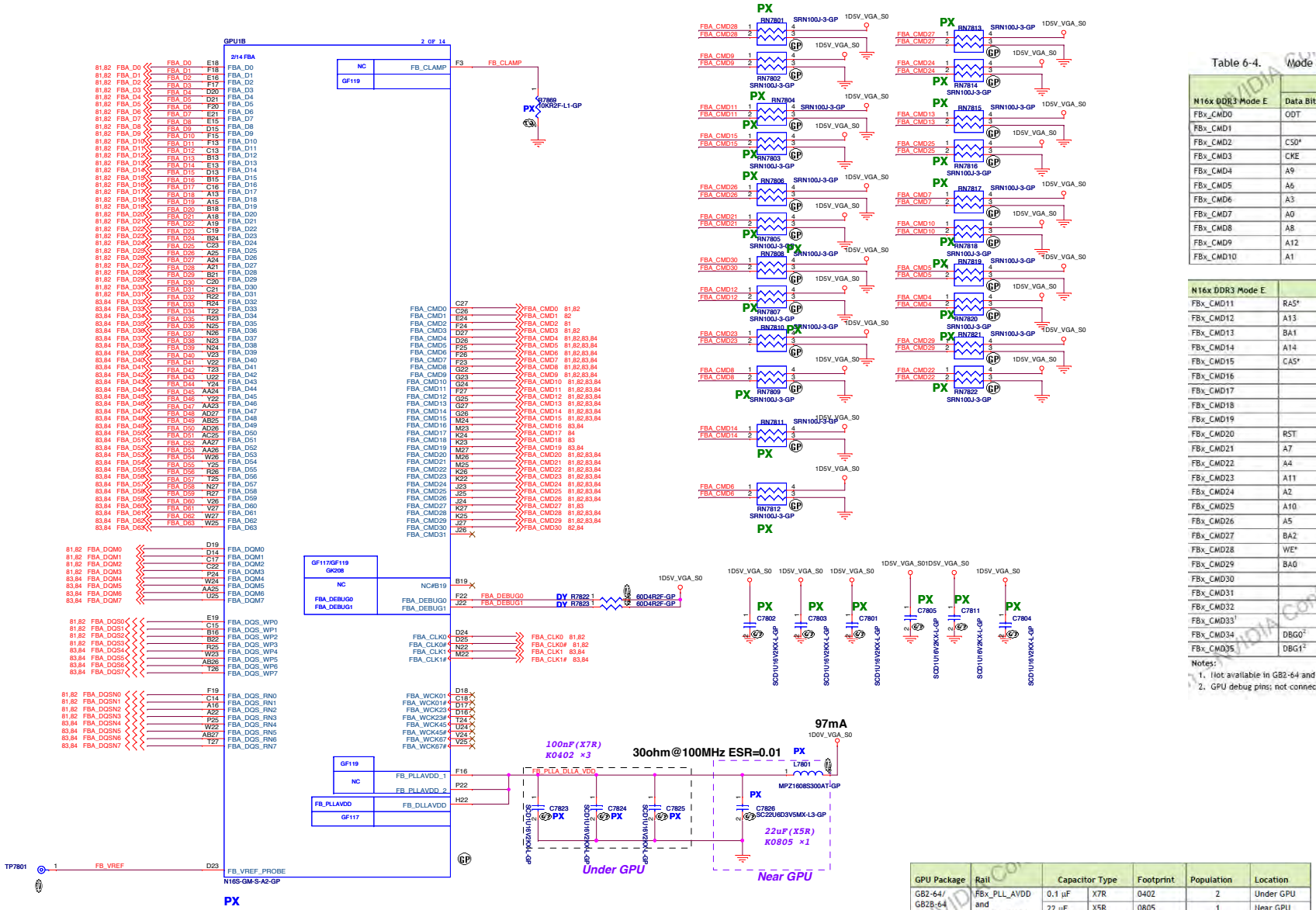


Table 6-4. Mode E Command Mapping

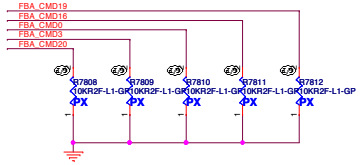
N16x DDR3 Mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2

N16x DDR3 Mode E	Rank 0		Rank 1	
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2
FBx_CMD31				
FBx_CMD32				
FBx_CMD33[1]				
FBx_CMD34	DBG0[2]			
FBx_CMD35	DBG1[2]			

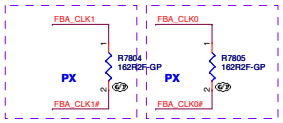
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 6.1.11.

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2-64/ GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Memory ODTx, CKEx and RST Termination



FBCLK Termination placed near each VRAM at board edge side



CHECK N16 Design guide P.98 Table 6-7

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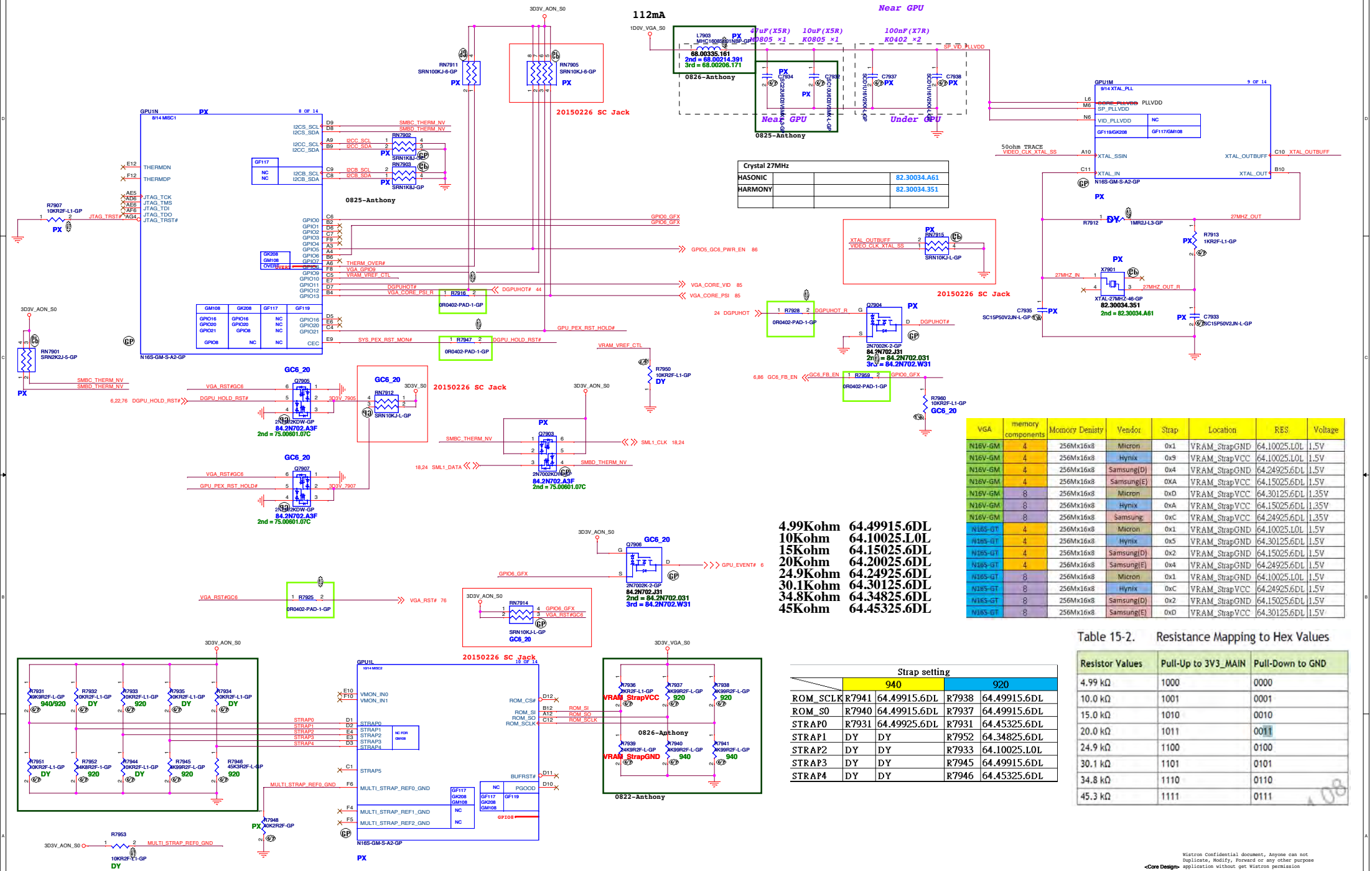

Crystal 27MHz			
HASONIC			82.30034.A61
HARMONY			82.30034.351

4.99Kohm	64.49915.6DL		
10Kohm	64.10025.L0L		
15Kohm	64.15025.6DL		
20Kohm	64.20025.6DL		
24.9Kohm	64.24925.6DL		
30.1Kohm	64.30125.6DL		
34.8Kohm	64.34825.6DL		
45Kohm	64.45325.6DL		

VGA	memory components	Momory Denisty	Vendor	Strap	Location	RES	Voltage
N16V-GM	4	256Mx16x8	Micron	0x1	VRAM_StrapGND	64.10025.L0L	1.5V
N16V-GM	4	256Mx16x8	Hynix	0x9	VRAM_StrapVCC	64.10025.L0L	1.5V
N16V-GM	4	256Mx16x8	Samsung(D)	0x4	VRAM_StrapGND	64.24925.6DL	1.5V
N16V-GM	4	256Mx16x8	Samsung(E)	0XA	VRAM_StrapVCC	64.15025.6DL	1.5V
N16V-GM	8	256Mx16x8	Micron	0xD	VRAM_StrapVCC	64.30125.6DL	1.35V
N16V-GM	8	256Mx16x8	Hynix	0xA	VRAM_StrapVCC	64.15025.6DL	1.35V
N16V-GM	8	256Mx16x8	Samsung	0xC	VRAM_StrapVCC	64.24925.6DL	1.35V
N16S-GT	4	256Mx16x8	Micron	0x1	VRAM_StrapGND	64.10025.L0L	1.5V
N16S-GT	4	256Mx16x8	Hynix	0x5	VRAM_StrapGND	64.30125.6DL	1.5V
N16S-GT	4	256Mx16x8	Samsung(D)	0x2	VRAM_StrapGND	64.15025.6DL	1.5V
N16S-GT	4	256Mx16x8	Samsung(E)	0x4	VRAM_StrapGND	64.24925.6DL	1.5V
N16S-GT	8	256Mx16x8	Micron	0x1	VRAM_StrapGND	64.10025.L0L	1.5V
N16S-GT	8	256Mx16x8	Hynix	0xC	VRAM_StrapVCC	64.24925.6DL	1.5V
N16S-GT	8	256Mx16x8	Samsung(D)	0x2	VRAM_StrapGND	64.15025.6DL	1.5V
N16S-GT	8	256Mx16x8	Samsung(E)	0xD	VRAM_StrapVCC	64.30125.6DL	1.5V

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Strap setting

	940		920	
ROM_SCLK	R7941	64.49915.6DL	R7938	64.49915.6DL
ROM_S0	R7940	64.49915.6DL	R7937	64.49915.6DL
STRAP0	R7931	64.49925.6DL	R7931	64.45325.6DL
STRAP1	DY	DY	R7952	64.34825.6DL
STRAP2	DY	DY	R7933	64.10025.L0L
STRAP3	DY	DY	R7945	64.49915.6DL
STRAP4	DY	DY	R7946	64.45325.6DL

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Size: A2 | Document Number: Brook_SLU | Rev: 1M

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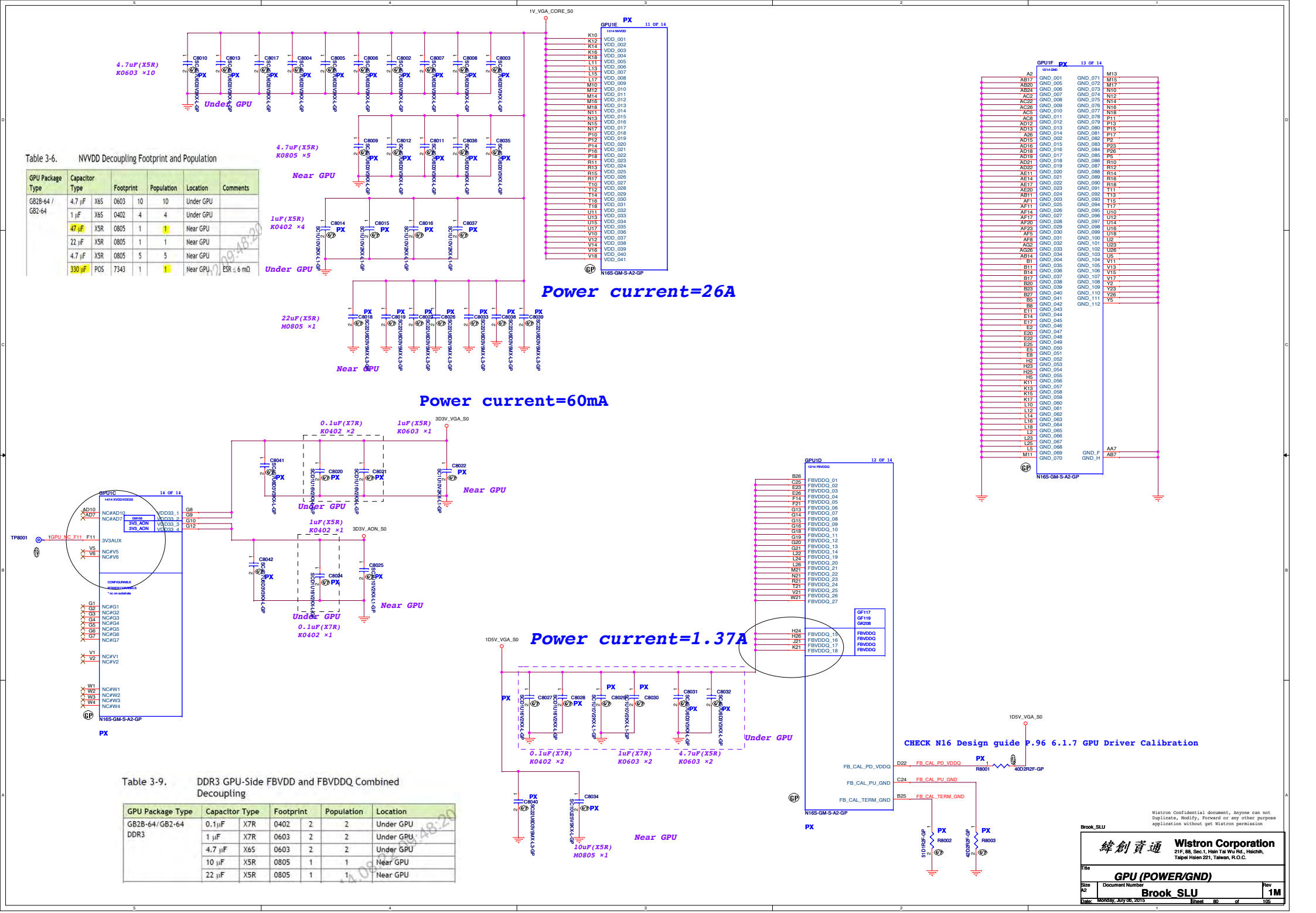
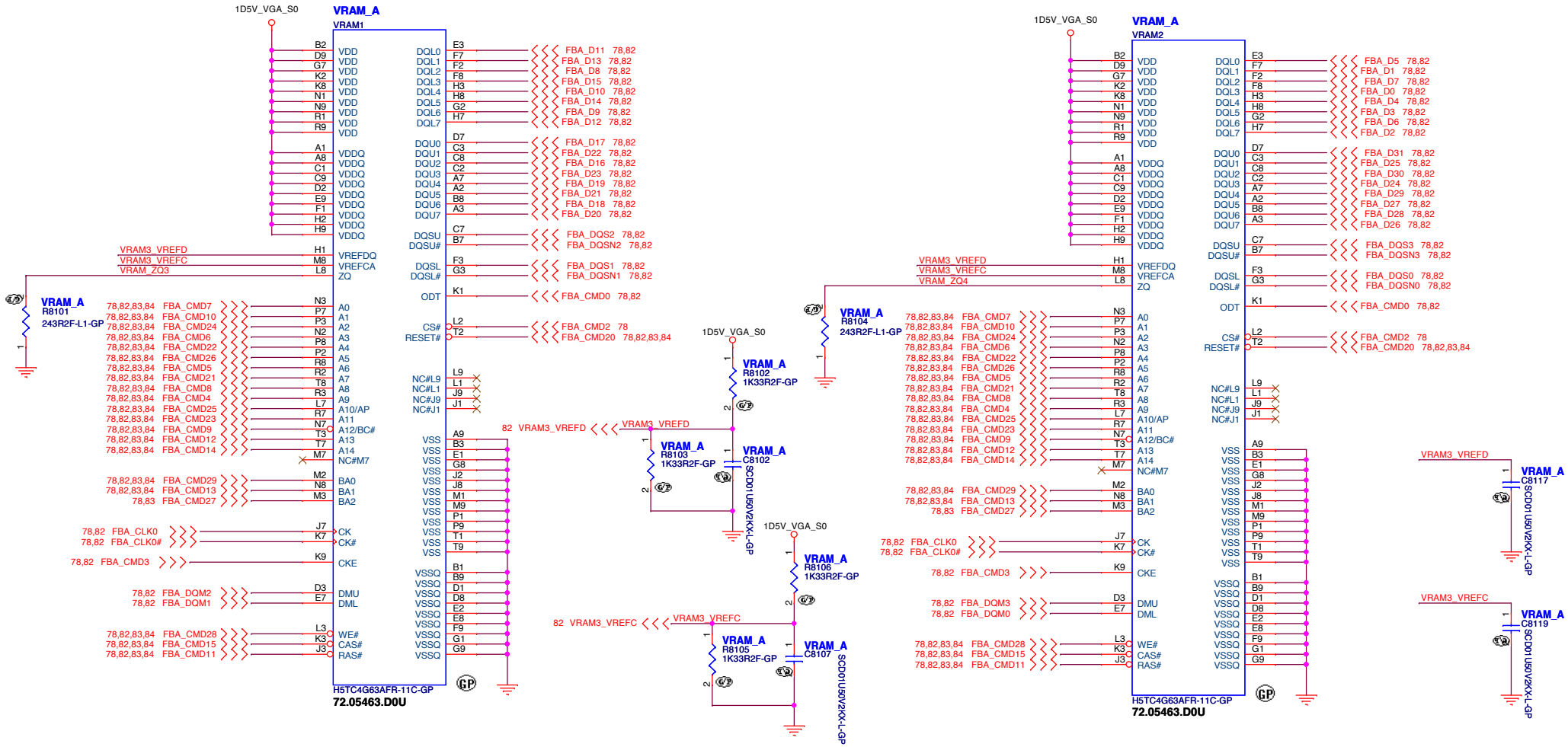


Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU



FOR VRAM1

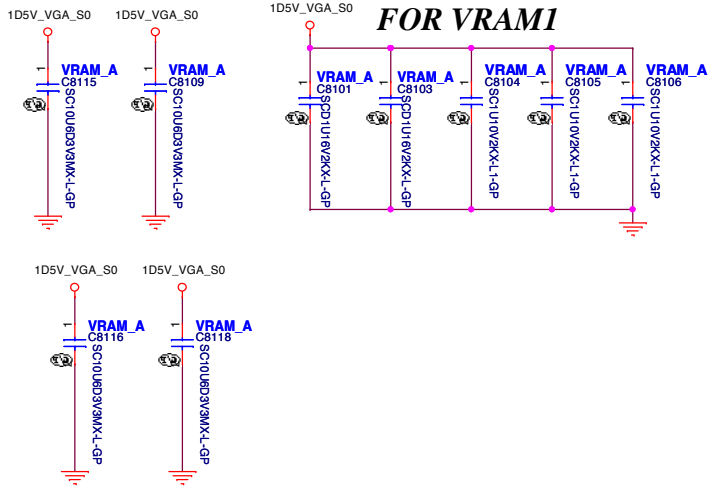
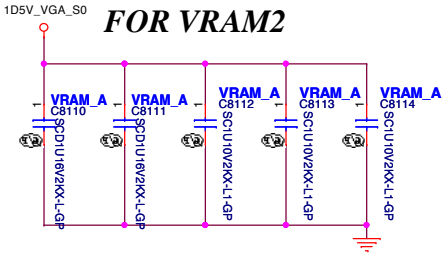


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

FOR VRAM2



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Title: GPU-VRA1,2 (1/4)

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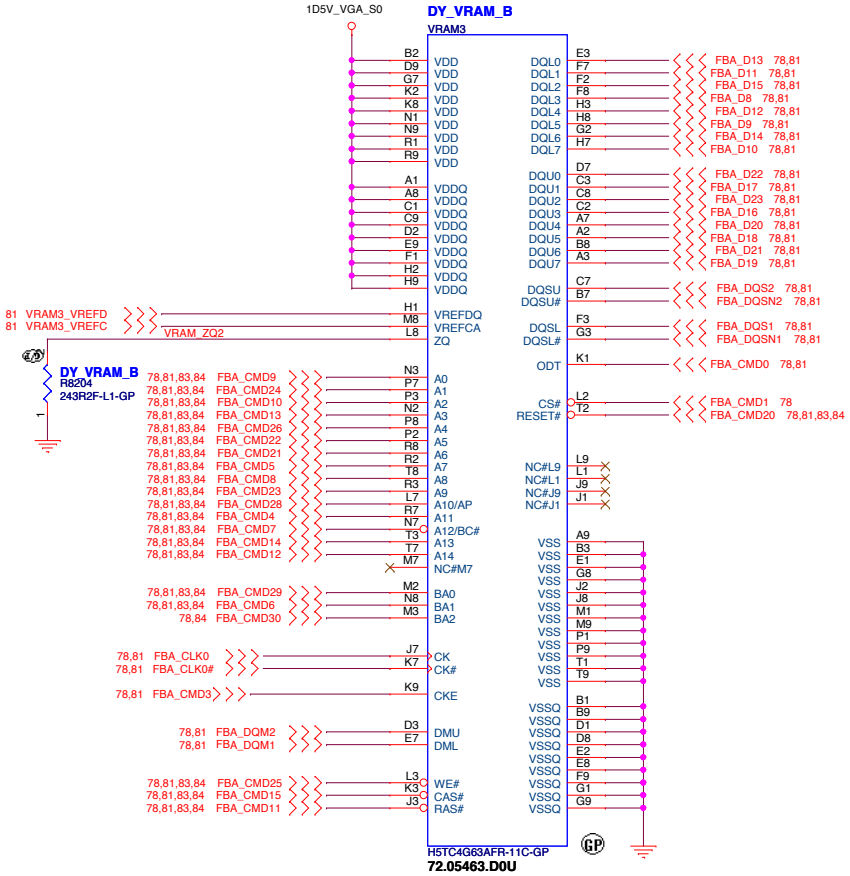
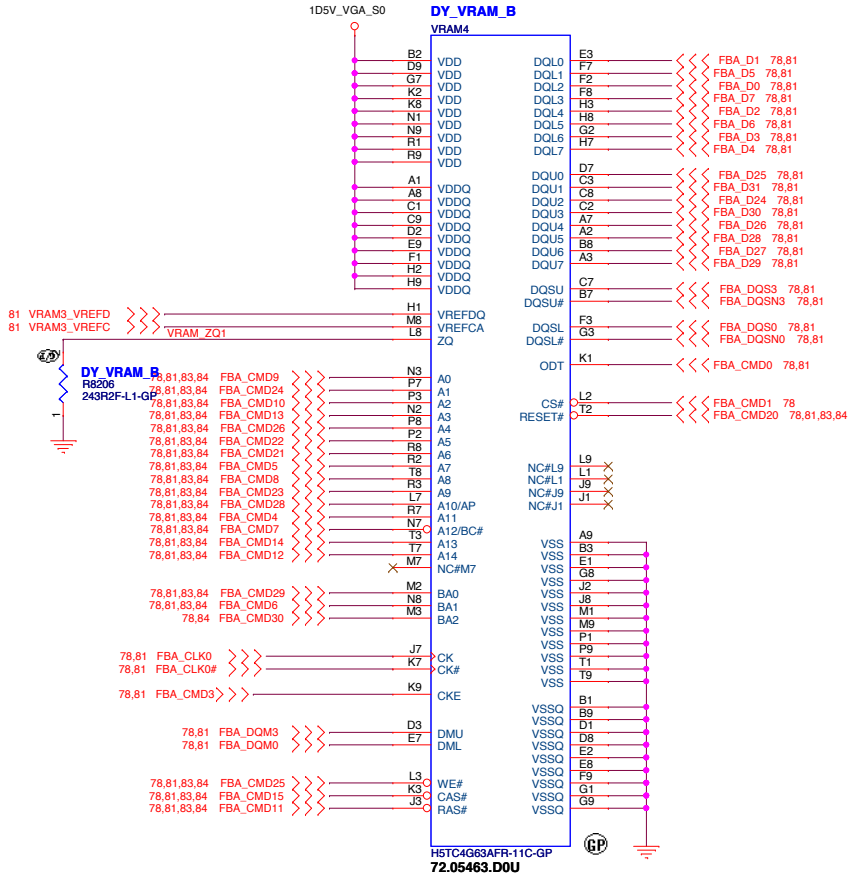
Date: Monday, July 06, 2015 | Sheet 81 of 105





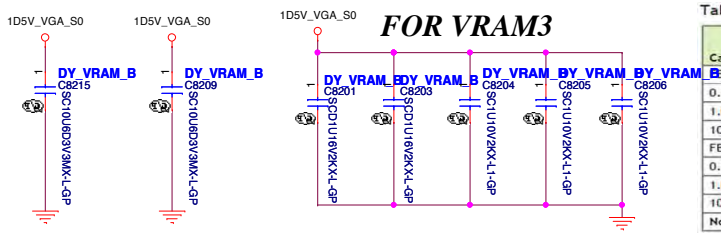
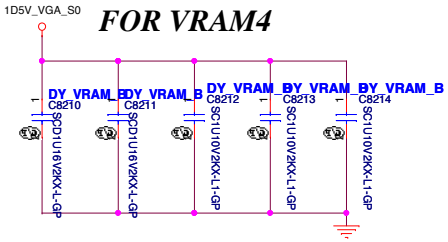
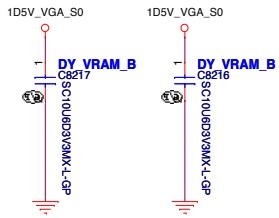


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.





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Title: GPU-VRAM3,4 (2/4)

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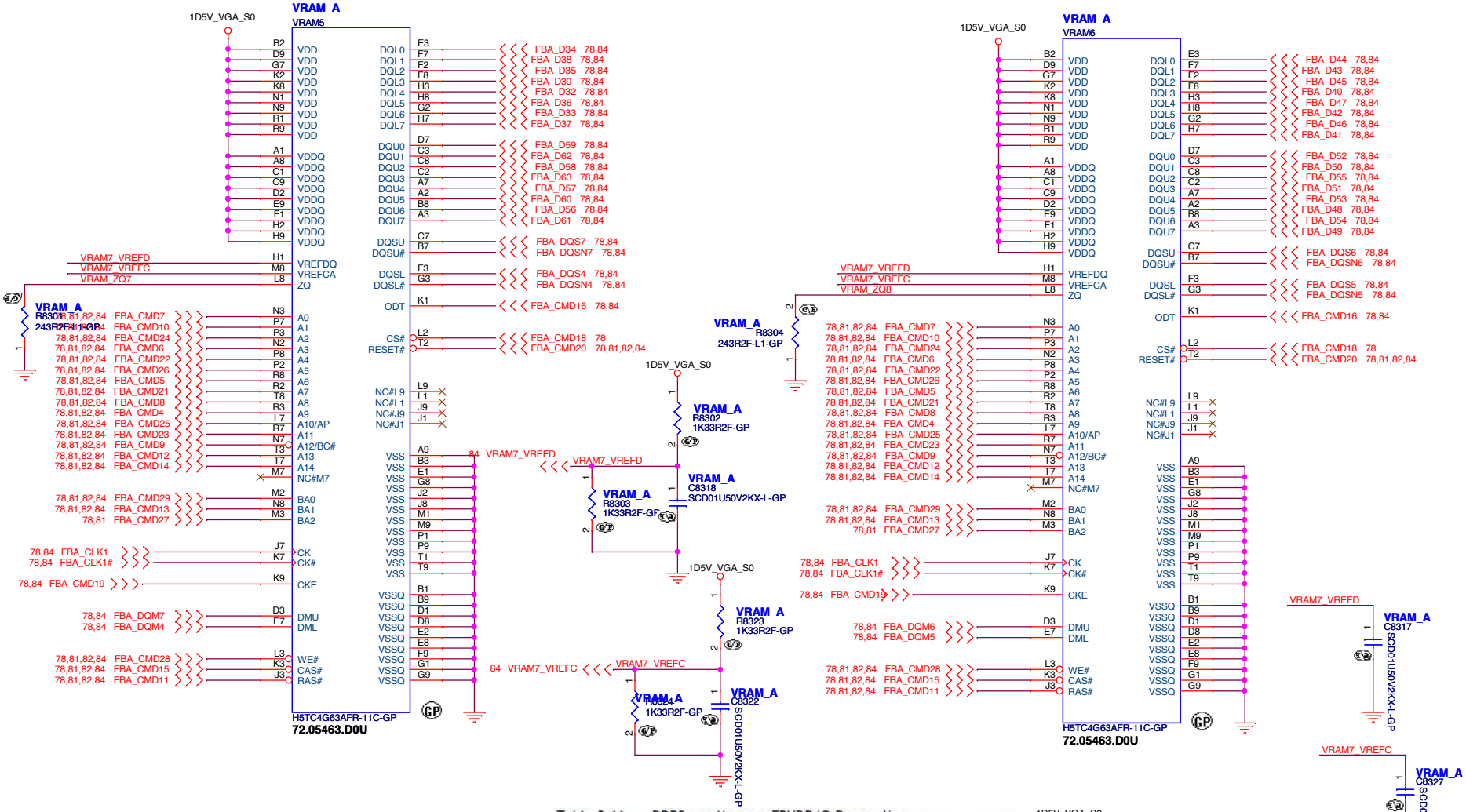
Date: Monday, July 06, 2015 | Sheet 82 of 105



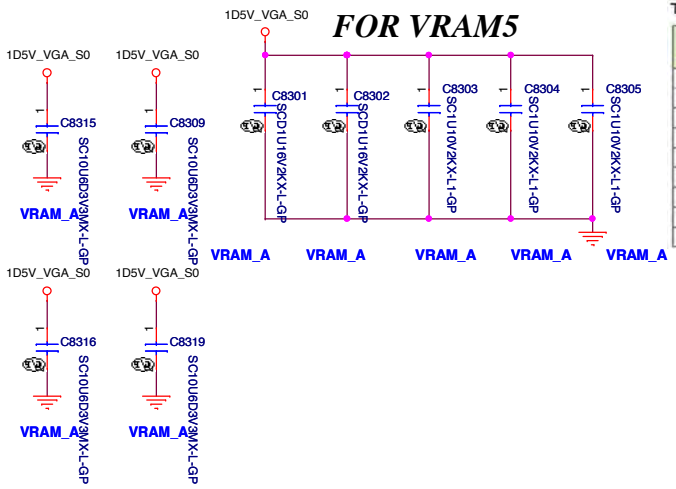
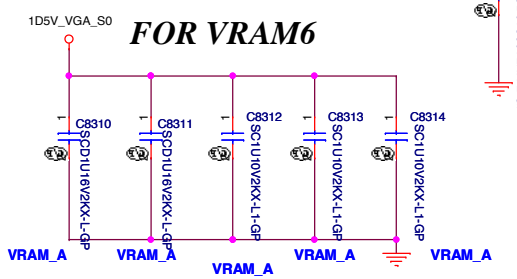


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



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Title: GPU-VRAM7,8 (4/4)

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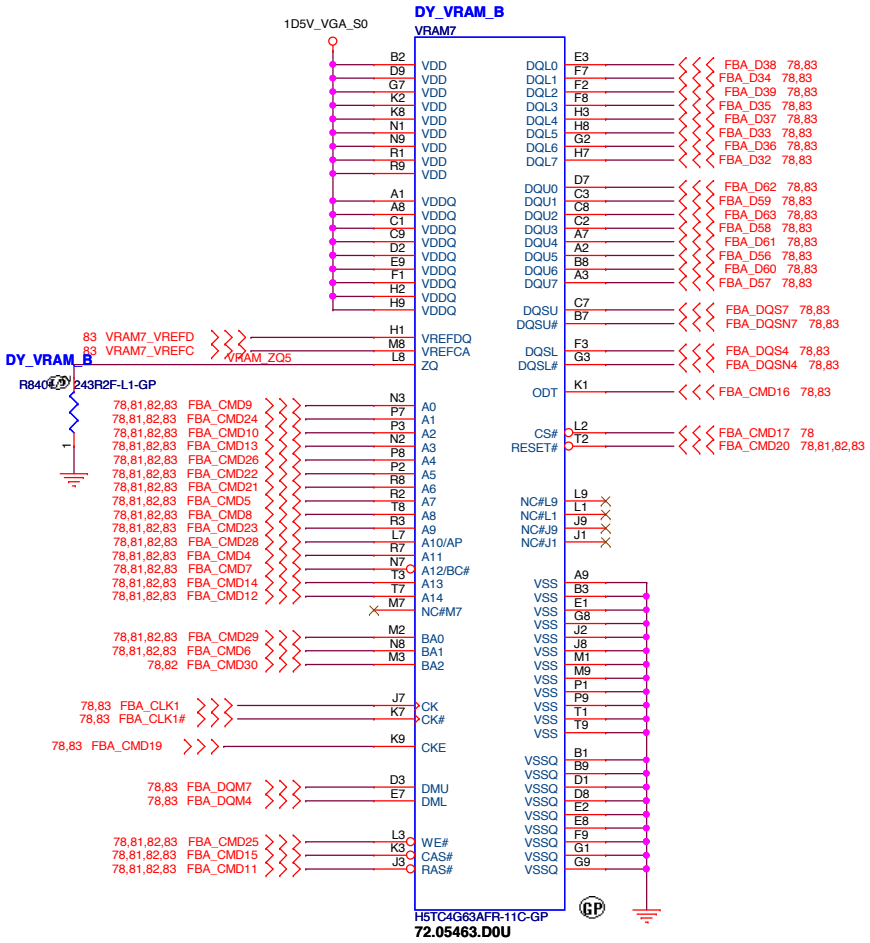
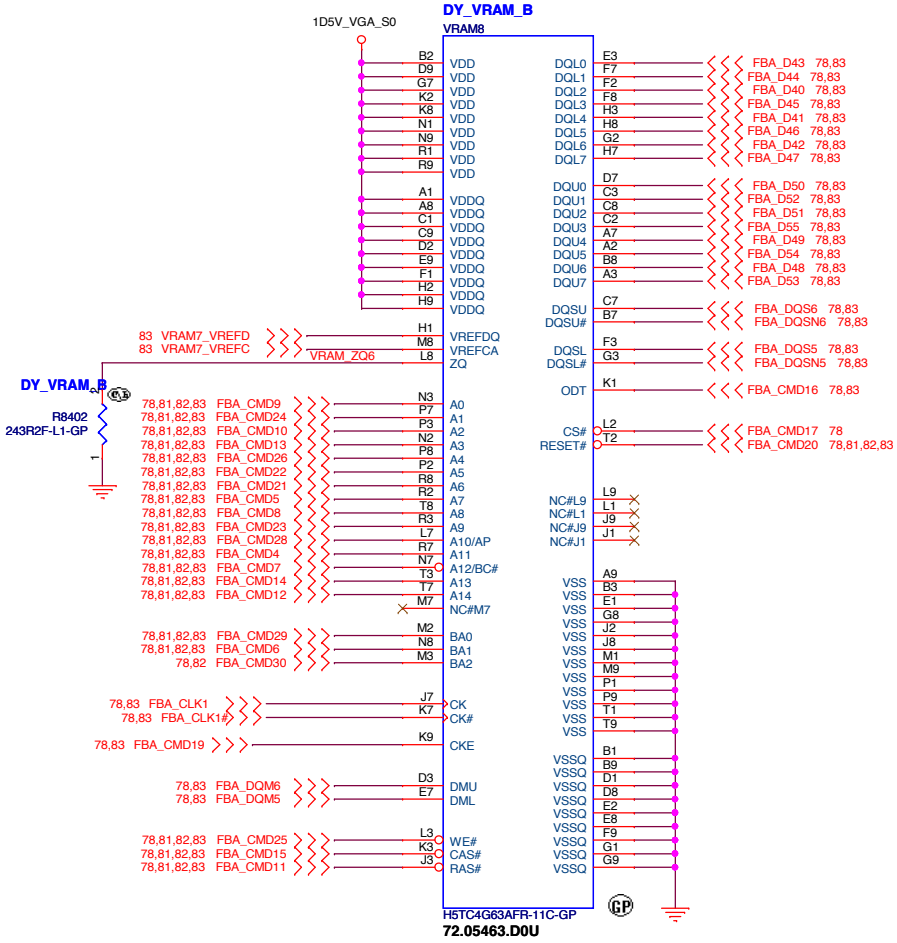




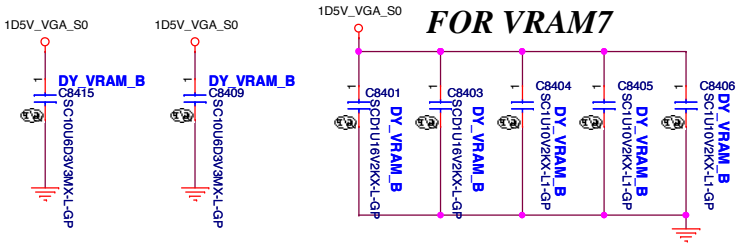
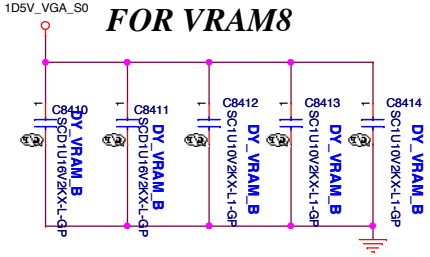
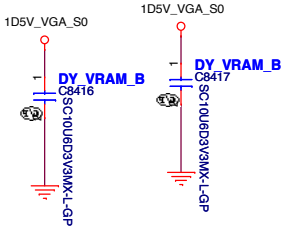


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separato					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.





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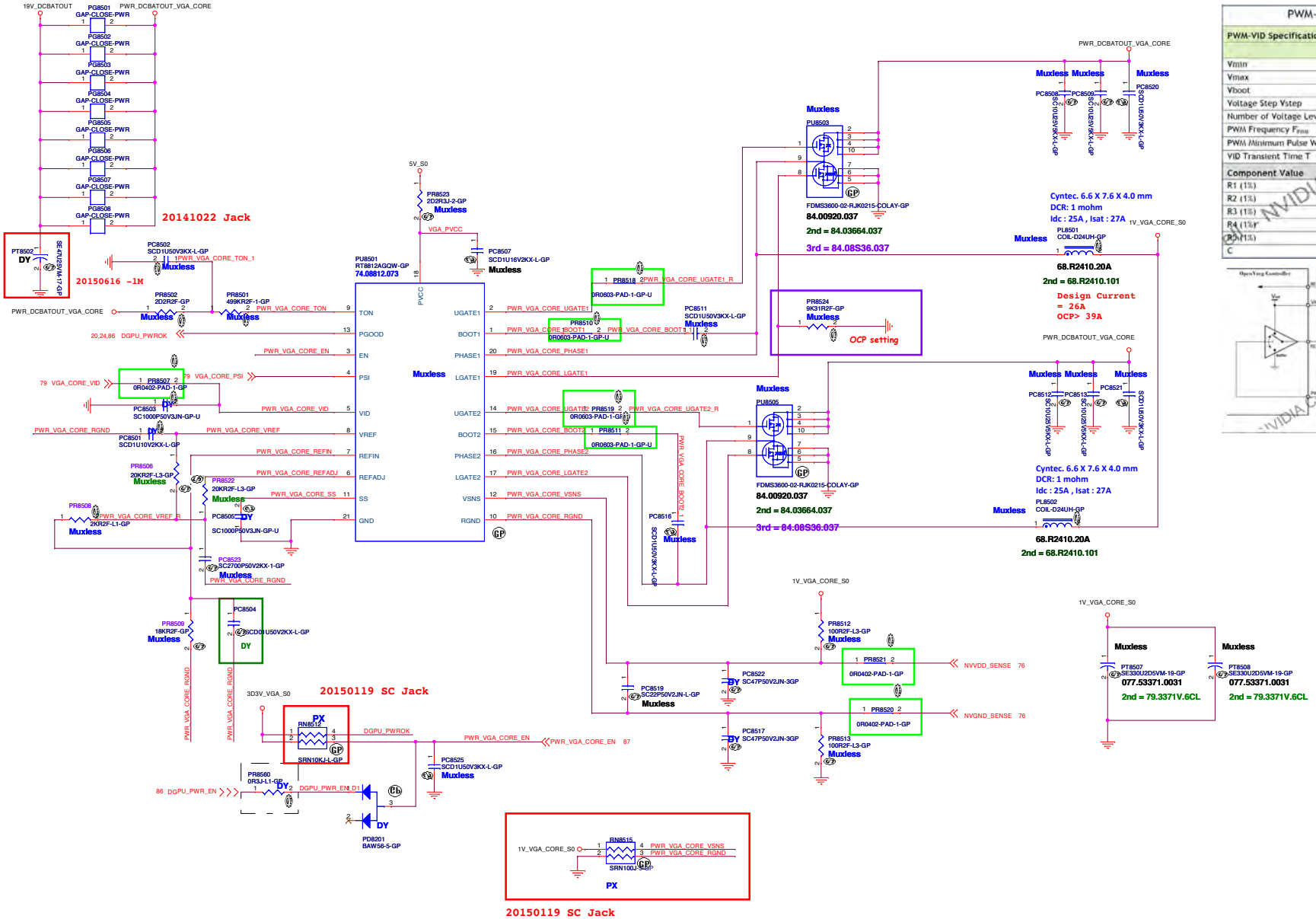
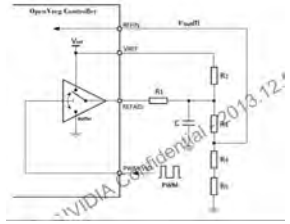
Title: GPU-VRAM7,8 (4/4)

Size: Custom | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 06, 2015 | Sheet 84 of 105



PWM-VID Spec and Component Values					
PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6



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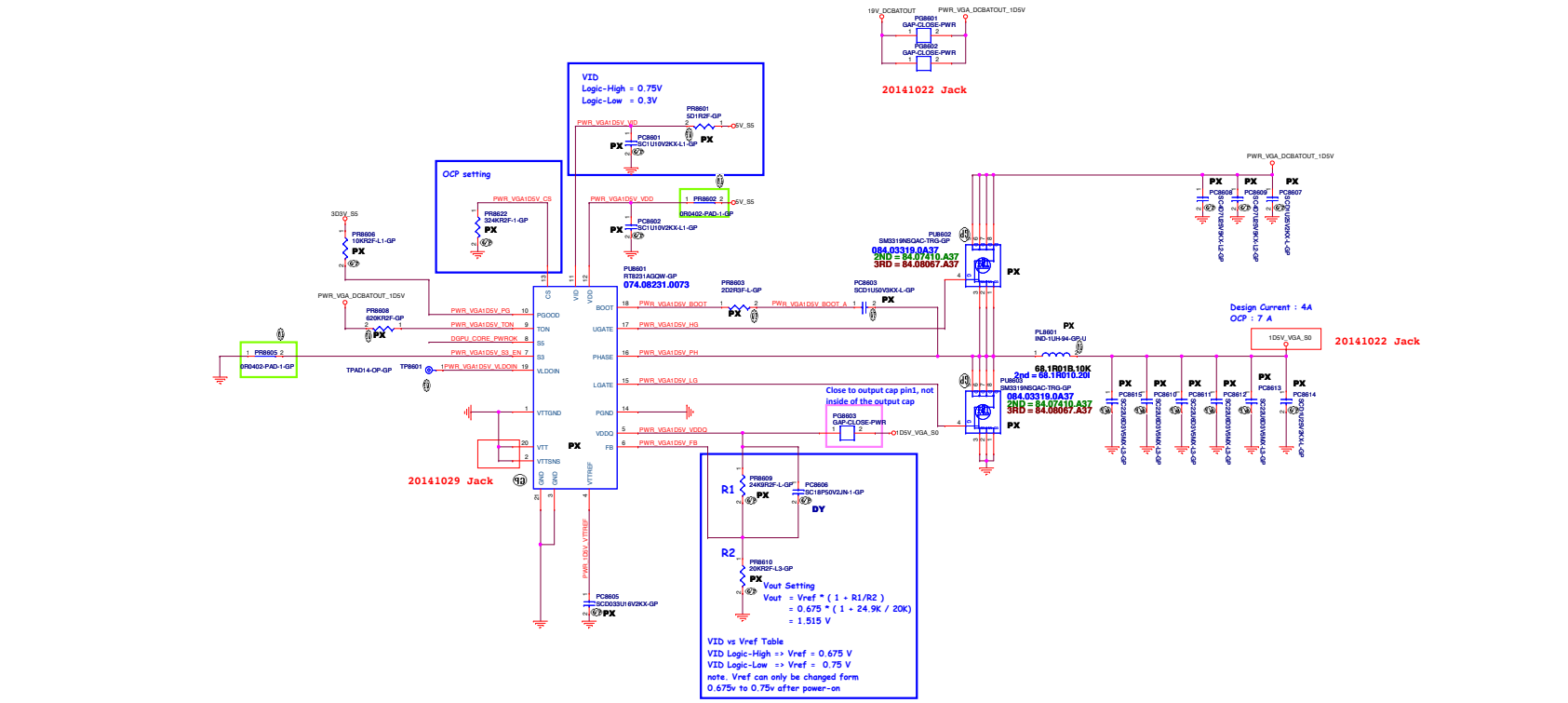
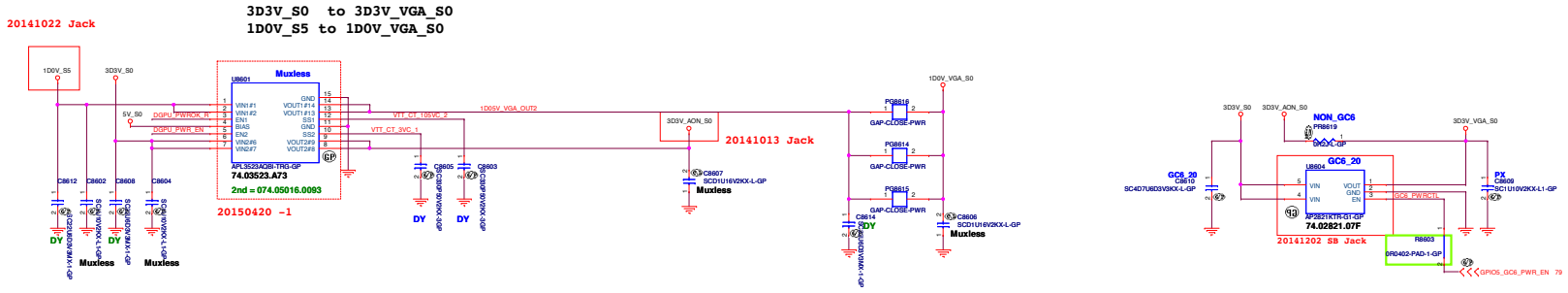
Title: VGA_CORE

Size: A2 | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 08, 2013 | Sheet 85 of 105

RT8231 for VGA_1D5V(For VRAM GDDR3)





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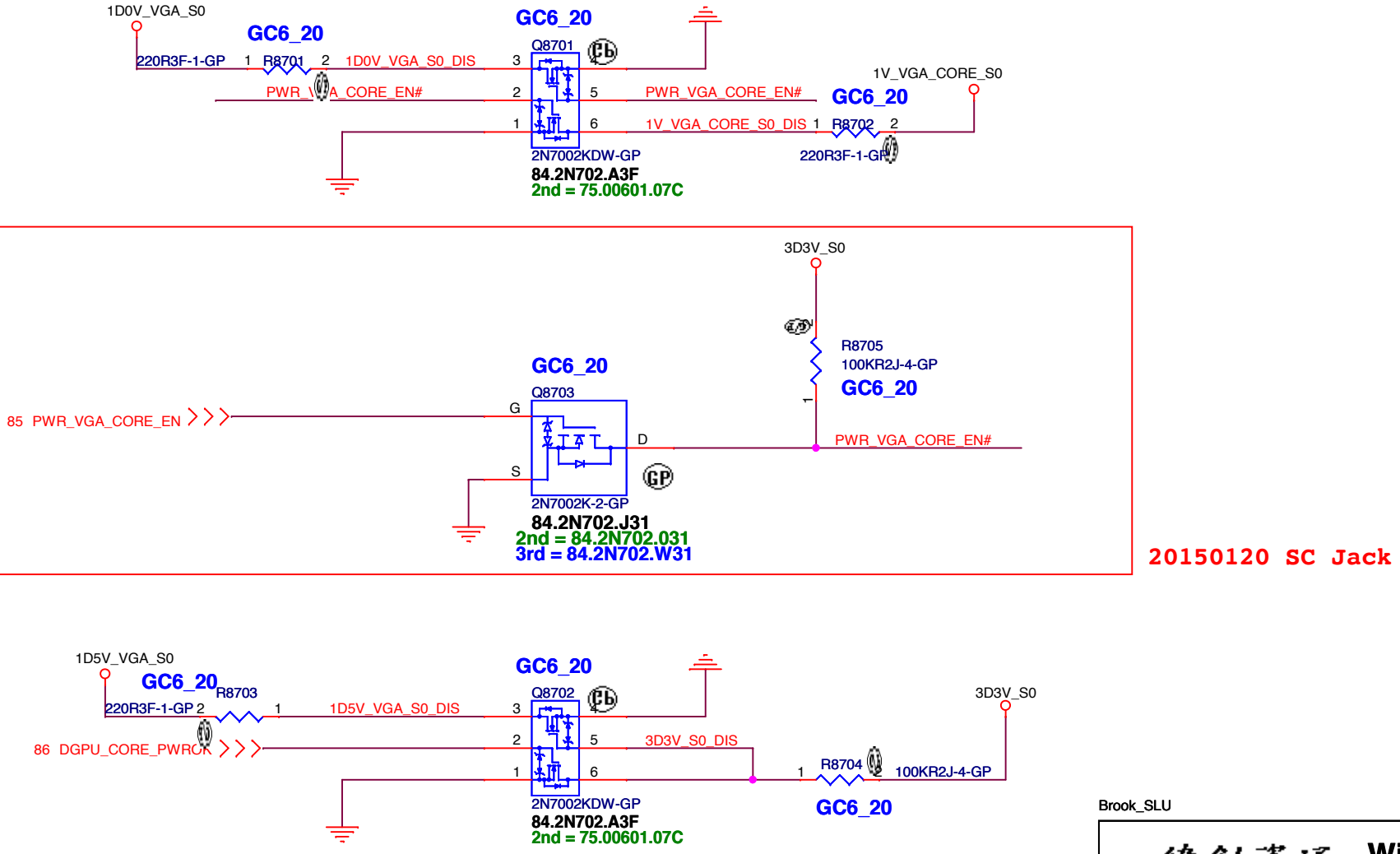
Title: DISCRETE VGA POWER

Size: Custom | Document Number: Brook_SLU | Rev: 1M

Date: Monday, July 08, 2013 | Sheet 86 of 105



20150120 SC Jack

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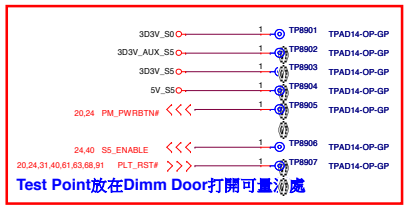
Check test point



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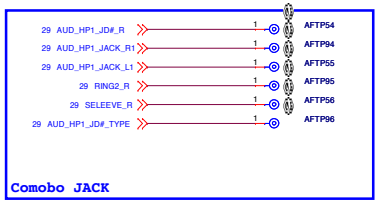

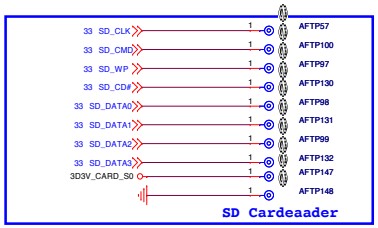

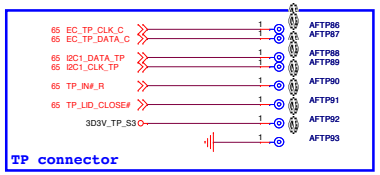

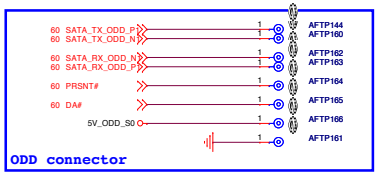

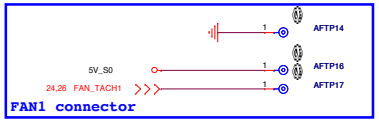

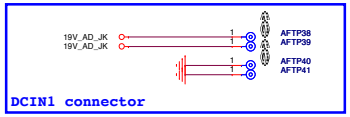

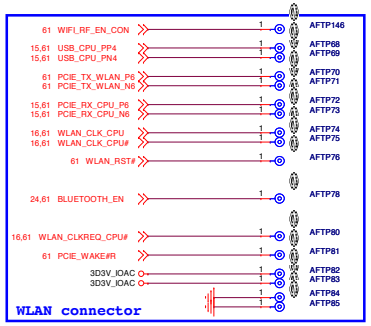

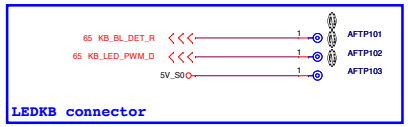

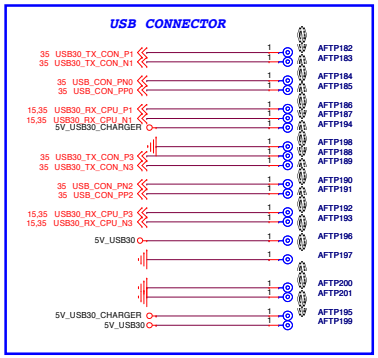

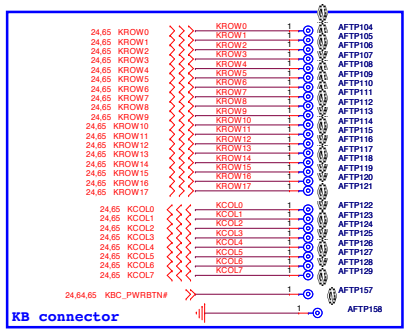

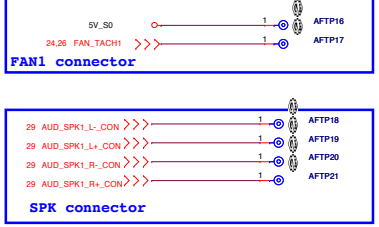

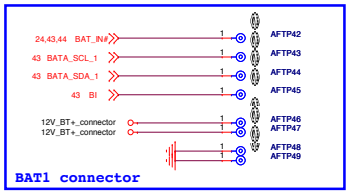

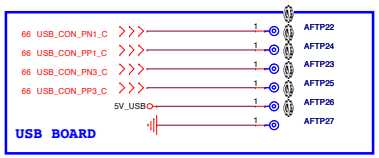

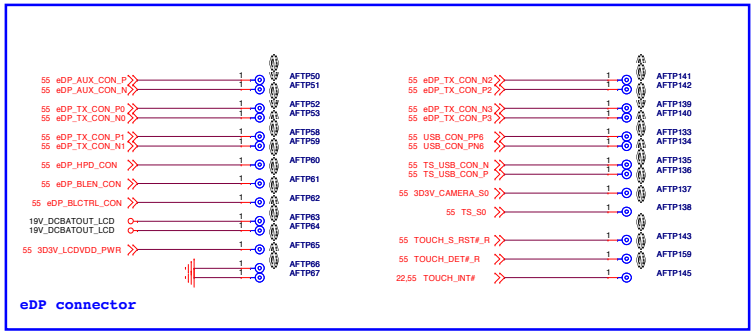

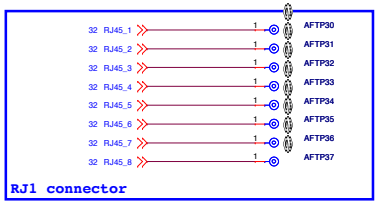

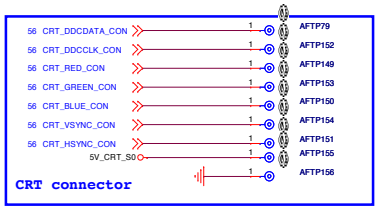

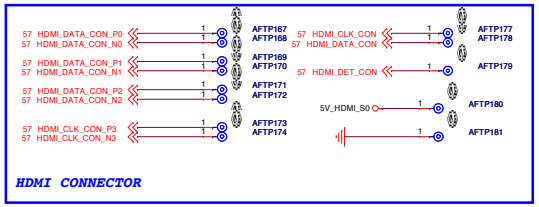

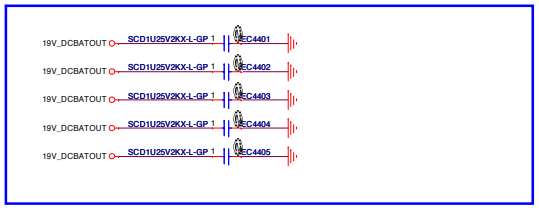

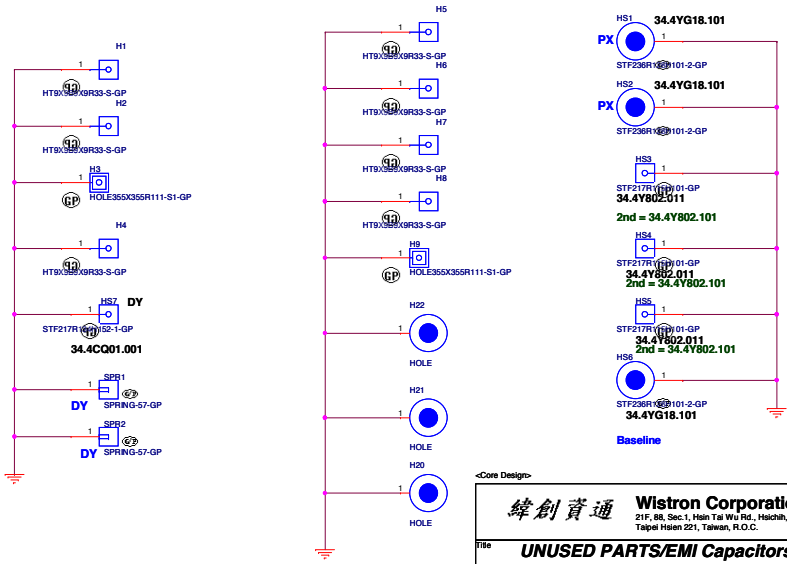

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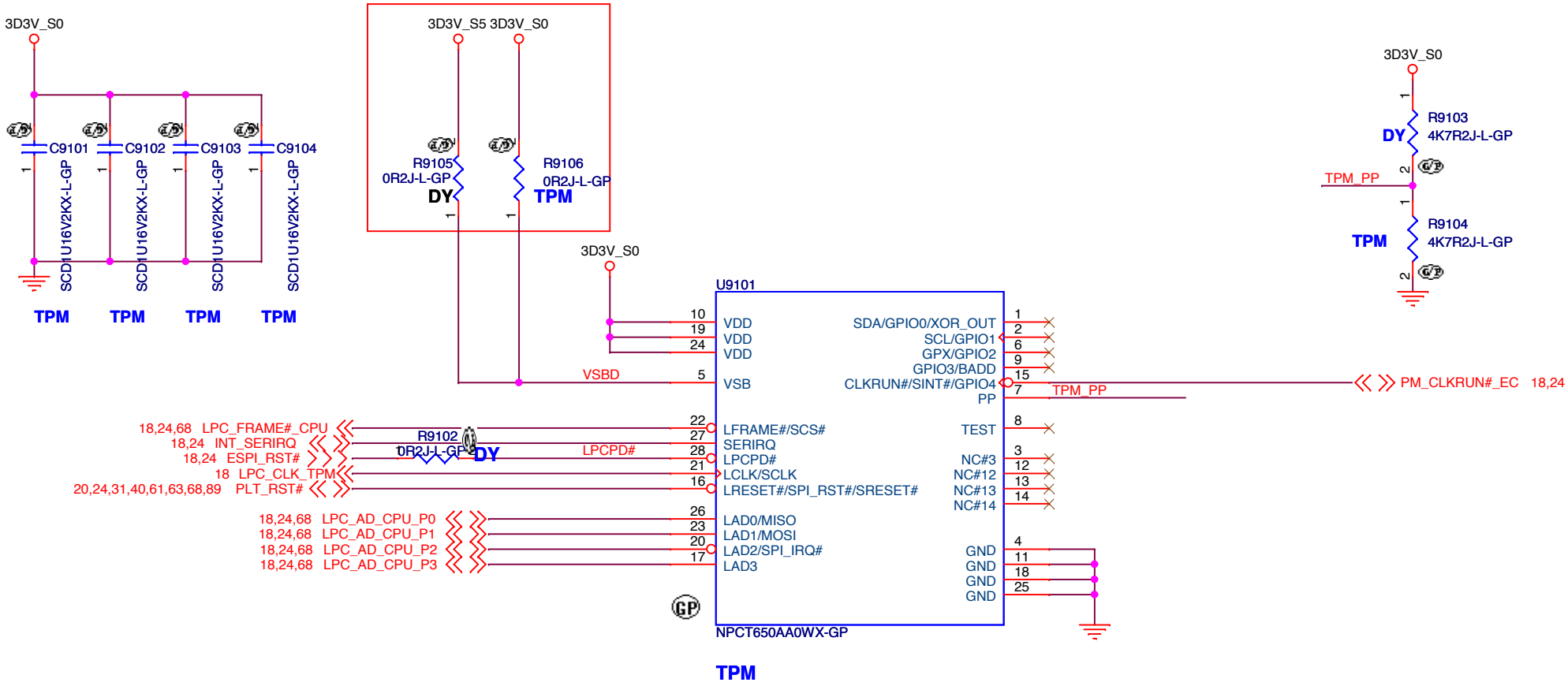

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Title **Smart Card socket**

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Title **Switchable GFX eDP**

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Title **Bottom Docking**

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Title: ***Inter LAN WG1217LM***

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Title	LAN Switch	
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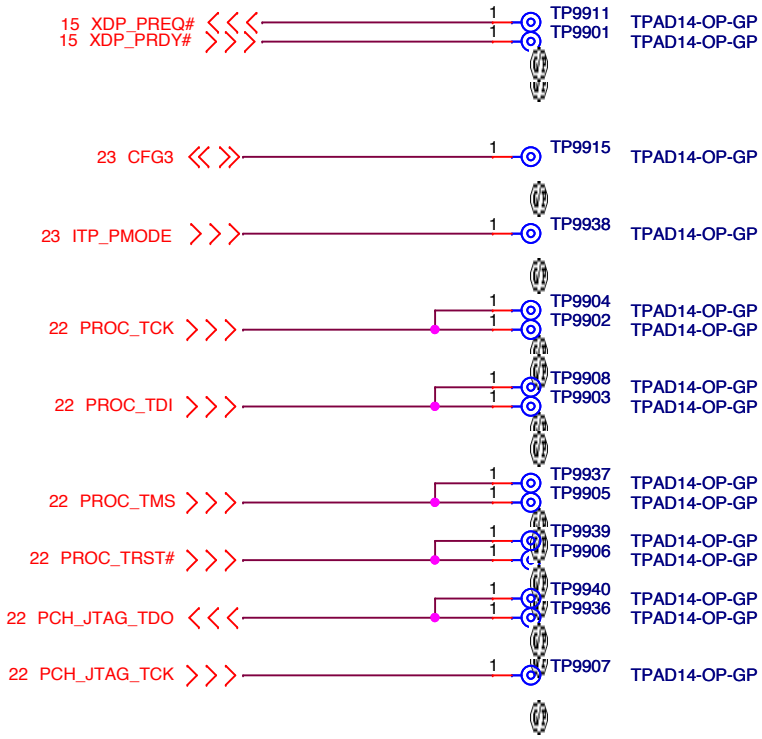
Main Func = Debug



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Title	***CPU_XDP***	
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Title: ***Change History***

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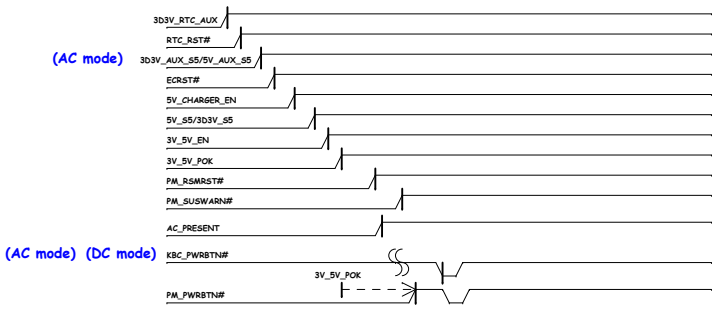
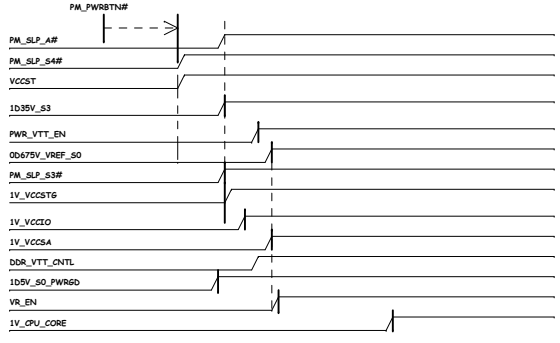
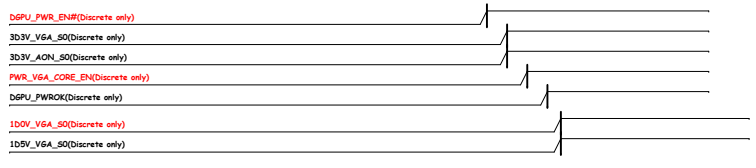
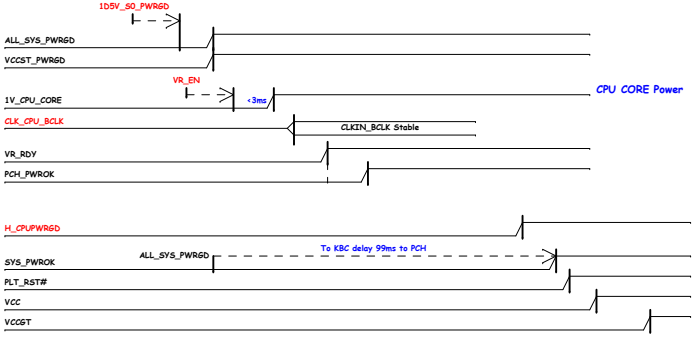
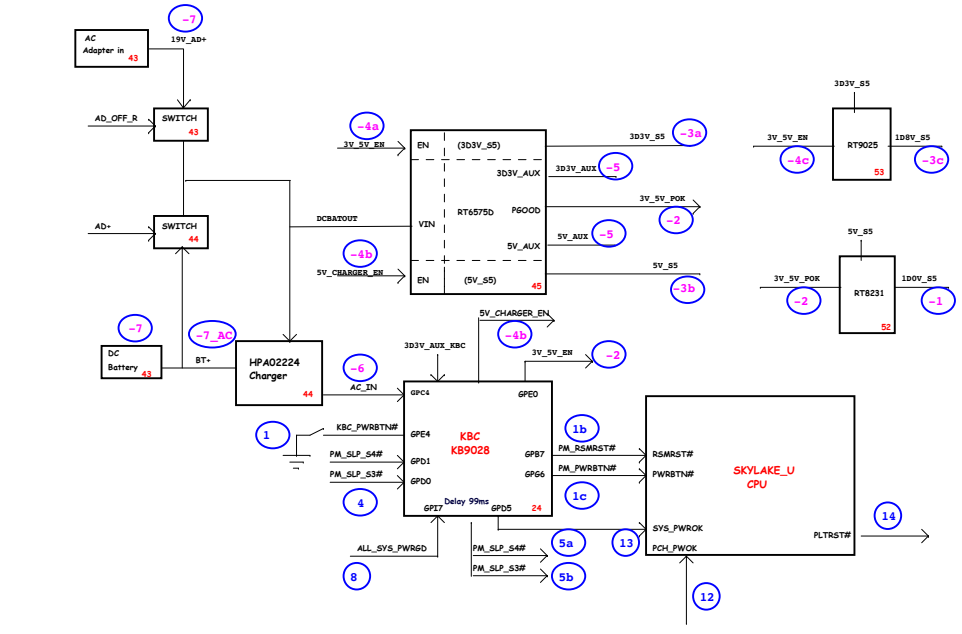
Intel-Power Up Sequence

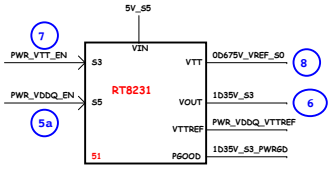


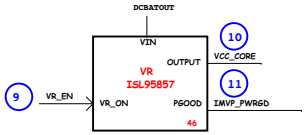


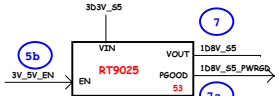


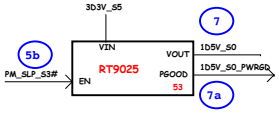


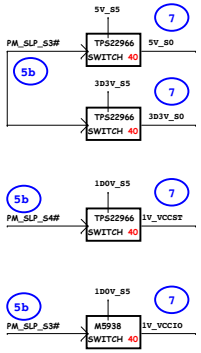


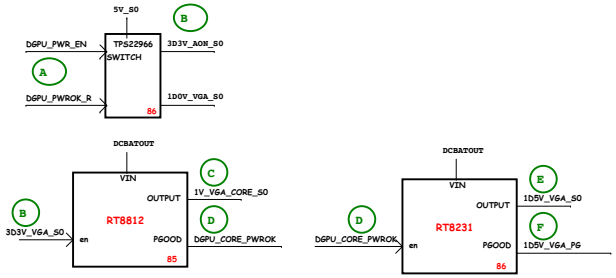












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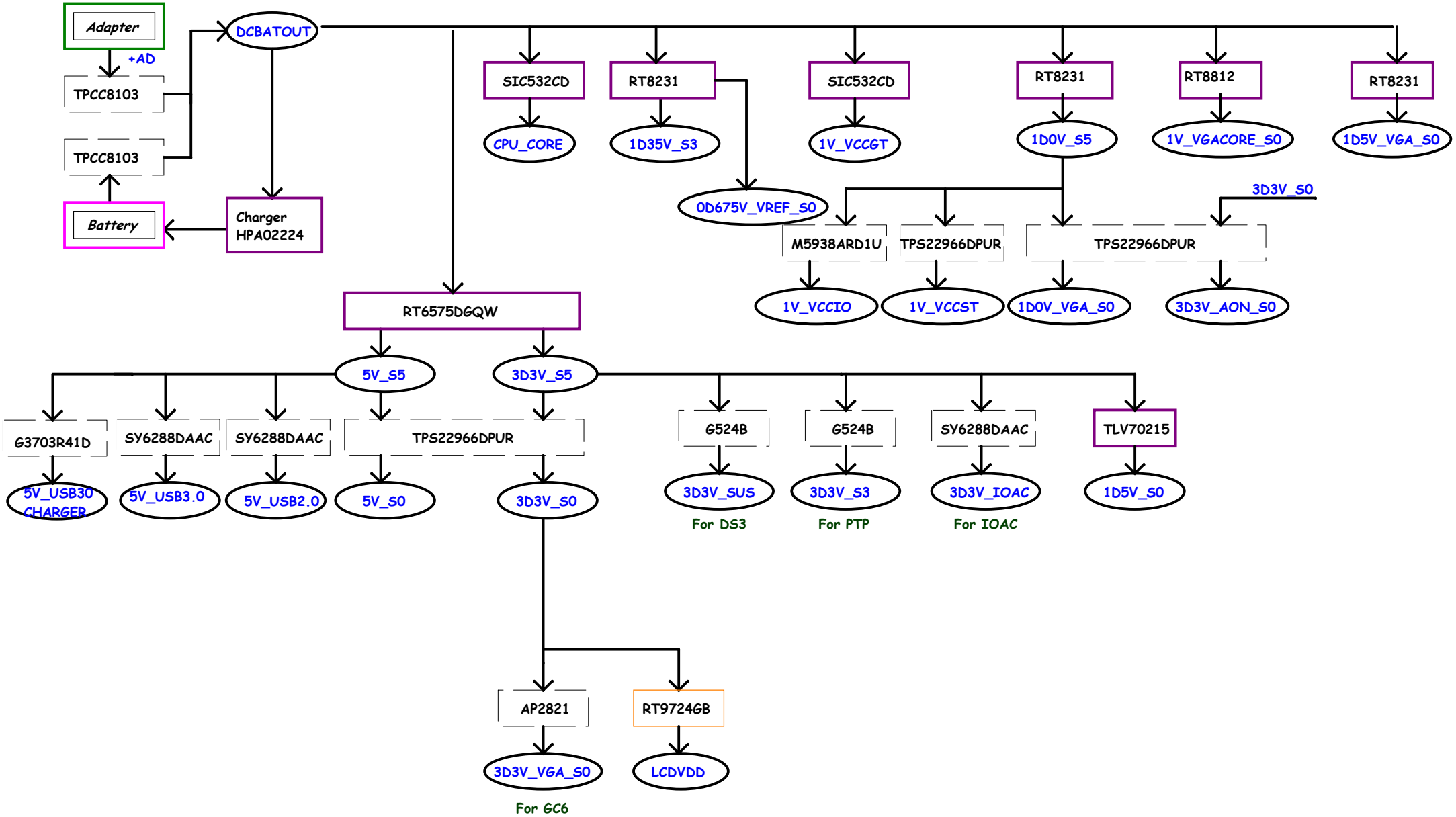

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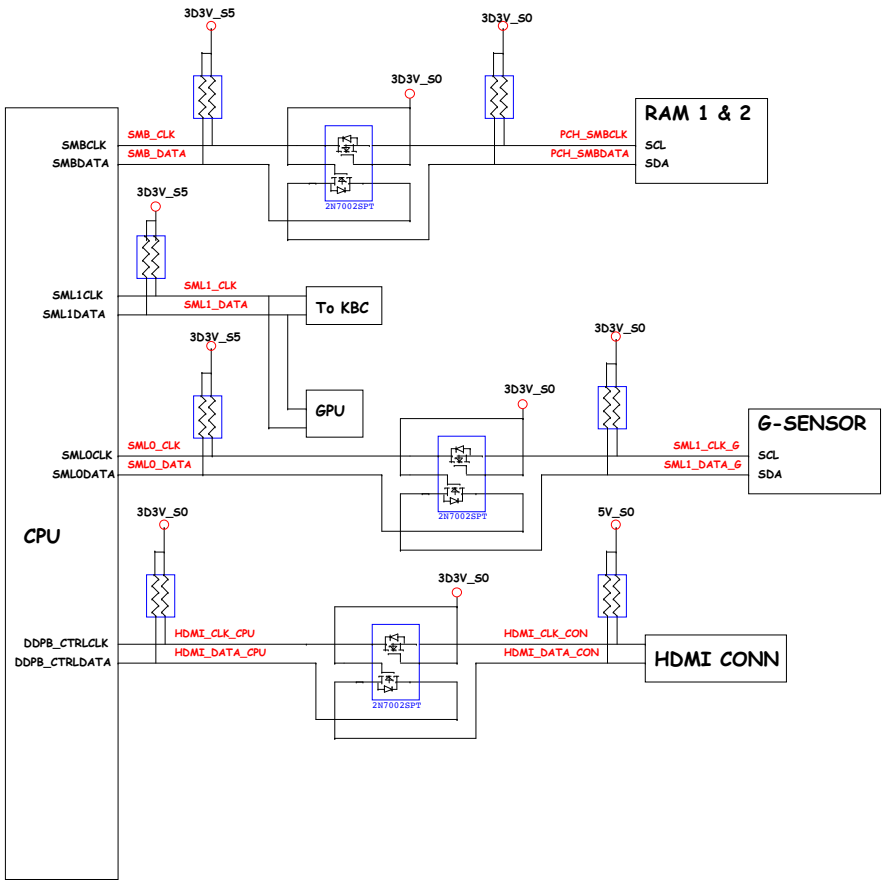
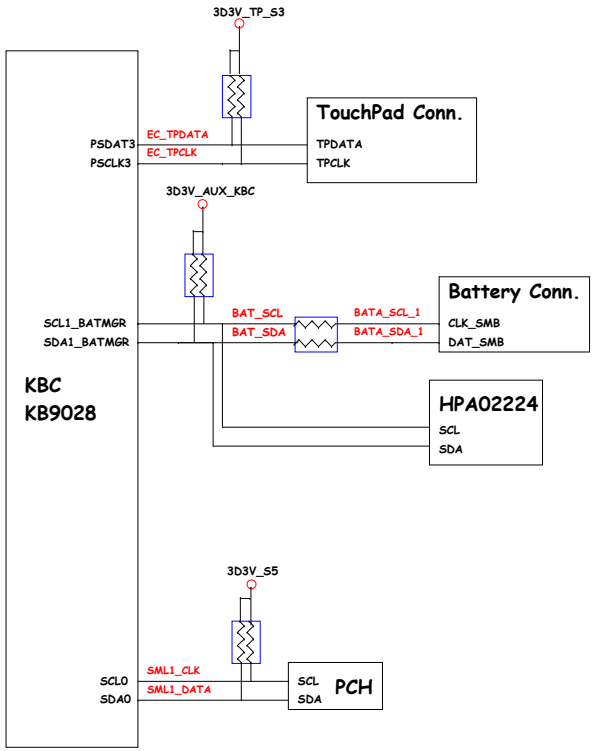
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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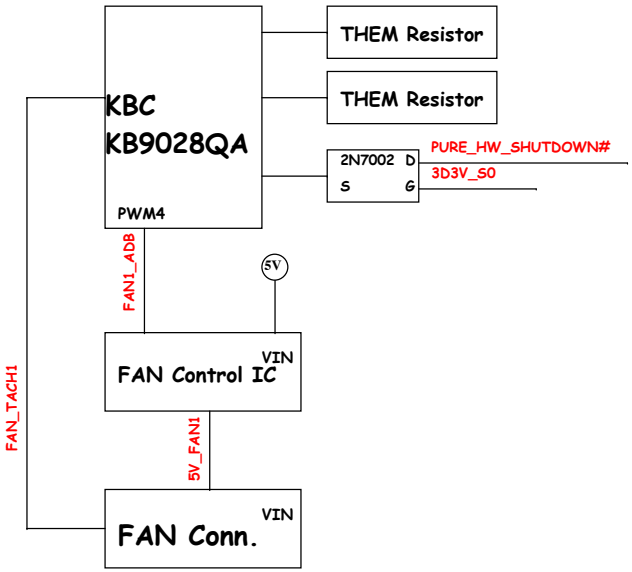
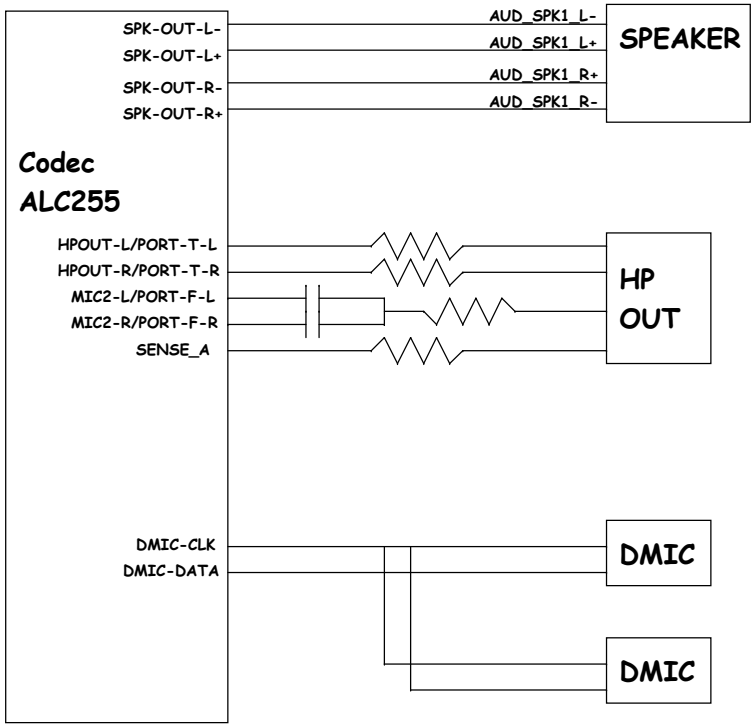
Thermal Block Diagram



Audio Block Diagram



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